# Soheil Salehi

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**Tenure-Track Assistant Professor** **Fall 2022-Present**
*ECE Department, University of Arizona, Tuscon, AZ*

**NSF-Sponsored Computing Innovation Fellow (CIFellow)** **Fall 2020-Fall 2022**
*ECE Department, University of California Davis, Davis, CA* *Mentor: Professor Houman Homayoun*
Associate Member, UC Davis Institute for Hardware and AI-enabled Cyber Security (IHACS)

## I. Technical Interests

Hardware and AI-enabled Security in IoT; Neuromorphic and Biologically-inspired AI Hardware; Energy-Efficient and Intelligent Signal Conversion and Processing in IoT; Reconfigurable and Adaptive Computer Architectures; Emerging Spin-Based Devices;

## II. Education

**Ph.D., Computer Engineering** **2014-2020**
*ECE Department, University of Central Florida, Orlando, FL* *Advisor: Dr. Ronald F. DeMara*
Dissertation: Energy-Efficient Signal Conversion and In-Memory Computing using Emerging Spin-based Devices

**M.S., Computer Engineering** **2014-2016**
*ECE Department, University of Central Florida, Orlando, FL* *Advisor: Dr. Ronald F. DeMara*
Thesis: Towards Energy-Efficient and Reliable Computing: From Highly-Scaled CMOS Devices to Resistive Memories

**B.S., Computer Engineering** **2009-2014**
*ECE Department, Isfahan University of Technology, Iran, (Visiting Student, University of Tehran, 2011-2014)*
Project: Design and implementation of Embedded Systems for Autonomous Vehicles using Wireless Sensor Networks

## III. Professional Experience

### A. Research Experience

***Privacy-Preserving, Intelligent, and Secure Embedded Systems (PRISMS) Lab*** **2022-Present**
*Assistant Professor* *ECE, University of Arizona*

- Developing neuromorphic computing accelerators for hardware security.
- Developing EDA tool flows for secure hardware design using Machine Learning.
- Developing novel and effective data-driven automated framework for hardware weakness and vulnerability prediction, detection, and mitigation recommendation utilizing Machine Learning and Natural Language Processing.
- Developing secure In-Memory Computing hardware accelerators.
- Developing security mechanisms to protect multitenant FPGAs from side-channel attacks.
- Prepare funding proposals for NSF, DARPA, DoD, NIH, DoE, etc.
- Advising and mentoring Ph.D., M.S., and B.S. students

***Institute for Hardware and AI-enabled Cyber Security (IHACS)*** **2021-2022**
*Associate Member* *ECE, University of California Davis*

- Seek to develop a theoretical basis for understanding the insider problem, and how existing techniques for detection, prevention, and remediation fit into such a framework.
- Aim to examining one of the most perplexing, and critical, problems today: how do we secure and assure the hardware supply chain?
- Propose to utilize the available vulnerability databases to describe the security holes at varying levels of detail and train an ML system to recognize vulnerabilities.
- Study the use of explainable AI to explain to developers and others how the vulnerabilities can be corrected.
- Aim to develop a new class of Hardware Security Module (HSM) using Neuromorphic Chips to enable high-throughput on-chip learning via established approaches for artificial neural network processing to provide run-time security.
- Hope to explore and develop novel software and hardware cyber security solutions for post-quantum security threats posed by the advanced quantum computing systems.
- Attempt to develop advanced security mechanisms to protect the supply chains of hardware and software components to ensure maximum security of both hardware and software components utilized within autonomous vehicles.
- Hope to develop educational materials related to hardware security and cyber security.
- Contributing to prepare funding proposals for NSF, DARPA, DoD, etc.

***Accelerated, Secure, and Energy-Efficient Computing (ASEEC) Lab*** **2020-2022**
*NSF-Sponsored CIFellow, Postdoctoral Research Fellow* *ECE, University of California Davis*

- Investigate security vulnerabilities within the IoT supply chain and demonstrate innovative use of supervised and unsupervised AI approaches to detect and prevent attacks on IoT hardware supply chain.
- Investigate possible hardware trojan insertion, firmware attack, and counterfeit component attack on Printed Circuit Boards (PCBs) within IoT supply chain.
- Demonstrate Firmware Attack coNstruction and Deployment on powEr Management IC (FANDEMIC) and its impacts on bare-metal IoT Applications.
- Investigate security vulnerabilities that exist within the Autonomous Vehicles' hardware.
- Trojan Resilience Untrusted Cell Library Analysis, Detection, and Mitigation.
- Demonstrate innovative use of supervised and unsupervised deep learning approaches to develop the proposed Deep-learning-based Power Side-channel Attacks (DeePSAs), which can accurately estimate the encryption key from sampled power traces even in the presence of process variation, signal noise, and perturbation.
- Demonstrate utilization of commercially available STT-MRAM to design energy and area optimized Look-Up Tables (LUTs) for the encryption hardware to mitigate the proposed DeePSA, called Secure Hardware for IoT using Emerging-devices against side-channeL Deep-learning attacks (SHIELD).
- Contributing to prepare funding proposals for NSF, DARPA, DoD, etc.
- Sub-Advising and mentoring Ph.D., M.S., and B.S. students

***Computer Architecture Lab (CAL)*** **2014-2020**
*Research Assistant* *ECE, University of Central Florida*

- Researched beyond von Neumann computing architectures for Internet of Things (IoT) devices and ambient-powered intelligent edge processing
- Designed mixed-signal circuits for energy-efficient signal conversion leveraging 2-terminal commercially-available STT-MTJs and 3-terminal emerging SOT-MTJs for digital memory storage and Analog-to-Digital Conversion applications
- Developed cross-layer algorithmic to hardware approaches for heterogeneous technology reconfigurable computing fabrics for in-situ signal processing
- Led student contributions to prepare funding proposals for NSF, DARPA, and SRC
- Sub-Advised and mentored Ph.D., M.S., and B.S. students

***Advanced Robotics and Intelligent Systems Lab*** **2013-2014**
*Research Assistant* *ECE Dept., University of Tehran*

- Conducted research on rehabilitation robotics and hardware design and implementation of intelligent robots

## B. Teaching Experience

**ECE413/513: Web Development and the Internet of Things** **Fall 2022**
*Instructor* *ECE Dept., University of Arizona*

- Teaching weekly lectures to 60+ students per semester; including grading assignments
- Designing and preparing project assignments, grading projects, and tutoring students via post-test remediation sessions
- Configuring and operating HTML, CSS, JavaScript, MongoDB, AWS, VSCode, and Embedded Programming

**EEL3801: Computer Organization and Design** **Fall 2014-Fall 2018**
*Lab Instructor* *ECE Dept., University of Central Florida*

- Sole recipient of the **Award for Excellence by a Graduate Teaching Assistant at the university-level**, 2015-2016
- Teaching weekly labs to 100+ students per semester; including grading assignments
- Designing and preparing project assignments, grading projects, and tutoring students via post-test remediation sessions
- Configuring and operating MARS Assembler and Xilinx ISE software and C/C++ and Verilog/VHDL Languages
- Preparing demonstration of processor RTL and Schematic design using Synopsys' Design Compiler

**Electronics I** **Spring 2013-Spring 2014**
*Teaching Assistant* *ECE Dept., University of Tehran*

**Theory of Formal Languages and Automata** **Fall 2013-Spring 2014**
*Teaching Assistant* *ECE Dept., University of Tehran*

**Microprocessors Interfacing Circuit Design** **Spring 2013, Spring 2014**
*Teaching Assistant* *ECE Dept., University of Tehran*

**Microprocessors** **Fall 2013**
*Teaching Assistant* *ECE Dept., University of Tehran*

**Advanced Programming and Laboratory** **Spring 2011**
*Lab Instructor* *ECE Dept., Isfahan University of Technology*

## C. Mentoring Experience

**Advising and Mentoring of Ph.D., M.S., and B.S. Students**
*Privacy-Preserving, Intelligent, and Secure Embedded Systems (PRISMS) Lab, University of Arizona*

1. Shahriar Golchin (Ph.D. Student)
2. Ayush Vaibhav Bhatti (M.S. Student)
3. Aeris El Asslouj (B.S. Student)
4. David Mazi (B.S. Student)

**Sub-Advising and Mentoring of Ph.D., M.S., and B.S. Students**
*Accelerated, Secure, and Energy-Efficient Computing (ASEEC) Lab, University of California Davis*

1. Gaurav Kolhe (Ph.D. Student)
2. Tyler Sheaves (Ph.D. Student)
3. Kevin Immanuel Gubbi (Ph.D. Student)
4. Ryan Tsang (Ph.D. Student)
5. Asmita Asmita (Ph.D. Student)
6. Han (Jane) Wang (Ph.D. Student)
7. Doreen Joseph (Ph.D. Student)
8. Rakibul Hassan (Ph.D. Student)
9. Sutej Kulkarni (M.S. Student)
10. Charan Bandi (M.S. Student)
11. Matthew Martel (B.S. Student)
12. Richard Ge (B.S. Student)

**Sub-Advising and Mentoring of Ph.D., M.S., B.S. Students**

*Computer Architecture Lab (CAL), University of Central Florida*

1. Hossein Pourmeidani (Ph.D. Student)
2. Shaadi Sheikhfaal (Ph.D. Student)
3. Mousam Hossain (Ph.D. Student)
4. Adrian Tatulian (Ph.D. Student)
5. Meghana Reddy Vangala (M.S. Student)
6. Harshit Gupta (M.S. Student)
7. Gustavo Camero (B.S. Student, NSF REU, Composed two IEEE Manuscripts, Ph.D. Student at CMU)
8. Adedoyin Adepegba (B.S. Student, NSF REU, Composed an IEEE Manuscript, Interning at Intel)
9. Paul Wood (B.S. Student, NSF REU, Composed an IEEE Manuscript, Interning at Intel)
10. Daniel Mulvaney (B.S. Student, NSF REU, Composed an IEEE Manuscript, Interning at L3Harris)

### D. Professional Training

**Computer Organization and Design** **Fall 2014-Fall 2018**

*Course Content Development* *University of Central Florida*

- Worked closely with two faculty members in order to develop Projects, Lab assignments, Quizzes, Exams, and Course Contents in an innovative electronically-delivered format for about 100 students per semester
- Designing and Preparing the course web page and online evaluation
- Developing a new method for lab assignments and lab assessments using Xilinx Basys2 FPGA boards
- Authoring a 14-Week Lab Manual for the required laboratory component

**Preparing Tomorrow's Faculty** **May 2015-August 2015**

*Academic Career Preparation Training Course (completed as a trainee)* *University of Central Florida*

- Creating and organizing course content and related documents
- Writing a teaching philosophy statement
- Identifying and discussing relevant issues in teaching and learning
- Managing students' behavior through effective policies and expectations
- Evaluating students' strengths related to teaching and learning
- Constructing a teaching portfolio

## IV. Publications (***Citations:404; H-Index:11; I-Index:17; Total:39; Journals:10; Conferences:29)***

### A. Journal Publications

*Total of 10 Journal Publications*

**i. Technical Manuscripts:**

8. K. Immanuel Gubbi, B. Saber Latibari, A. Srikanth, T. Sheaves, S. A. Beheshti-Shirazi, S. Manoj P. D., S. Rafatirad, A. Sasan, H. Homayoun, and **S. Salehi**, "Hardware Trojan Detection using Machine Learning: A Tutorial," *ACM Transactions on Embedded Computing Systems*, accepted, 2022. (Impact Factor: 1.886)

7. **S. Salehi**, and R. F. DeMara, "Adaptive Non-Uniform Compressive Sensing using SOT-MRAM Multibit Crossbar Arrays," *IEEE Transactions on Nanotechnology (TNANO)*, vol. 20, pp. 224-228, 2021. (Impact Factor: 2.57)

6. **S. Salehi**, and R. F. DeMara, "SLIM-ADC: Spin-based Logic-In-Memory Analog to Digital Converter Leveraging SHE-enabled Domain Wall Motion Devices," *Microelectronics Journal*, vol. 81, pp. 137-143, 2018. (Impact Factor: 1.605)
**Special Issue on "Spintronic Integrated Circuits and New Architectures for Low Power Electronics"**

5. **S. Salehi**, M. Boloursaz Mashhadi, A. Zaeemzadeh, N. Rahnavard, and R. F. DeMara, "Energy-Aware Adaptive Rate and Resolution Sampling of Spectrally Sparse Signals Leveraging VCMA-MTJ Devices," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, vol. 8, no. 4, pp. 679-692, 2018. (Impact Factor: 3.916)
**Special Issue on "Energy-Quality Scalable Circuits and Systems"**

4. **S. Salehi**, N. Khoshavi, R. Zand, and R. F. DeMara, "Self-Organized Sub-bank SHE-MRAM-based LLC: an Energy-Efficient and Variation-Immune Read and Write Architecture," *Integration, The VLSI Journal*, vol. 65, pp. 293-307, 2019. (Impact Factor: 1.211)
**Special Issue on "International Symposium on Quality Electronic Design (ISQED) 2017"**

3. **S. Salehi**, N. Khoshavi, and R. F. DeMara, "Mitigating Process Variability for Non-Volatile Cache Resilience and Yield," *IEEE Transactions on Emerging Topics in Computing (TETC)*, vol. 8, no. 3, pp. 724-737, July-September, 2020. (Impact Factor: 7.691)
**Special Issue on "Reliability-aware Design and Analysis Methods for Digital Systems: from Gate to System Level"**

2. **S. Salehi**, D. Fan, and R. F. DeMara, "Survey of STT-MRAM Cell Design Strategies: Taxonomy and Sense Amplifier Tradeoffs for Resiliency," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 13, no. 3, pp. 1-16, 2017. (Impact Factor: 1.42)

1. R. Zand, A. Roohi, **S. Salehi**, and R. F. DeMara, "Scalable Adaptive Spintronic Reconfigurable Logic using Area-Matched MTJ Design," *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, vol. 63, no. 7, pp. 678-682, 2016. (Impact Factor: 3.292)

**ii. STEM Educational Manuscripts:**

2. R. F. DeMara, **S. Salehi**, R. Hartshorne, B. Chen, and E. Saqr, "Observable, Traceable, Auto-graded Computer-Mediated Collaborative Learning," *Journal of Interactive Learning Research (JILR)*, vol. 30, no. 3, pp. 397-424, September 2019.

1. B. Chen, R. F. DeMara, **S. Salehi**, and R. Hartshorne, "Elevating Learner Engagement and Outcomes using In-Situ Online Formative Assessment in the Engineering Laboratory: A Viable Alternative to Weekly Lab Reports," *IEEE Transactions on Education*, vol. 61, no. 1, pp. 1-10, February 2018. (Impact Factor: 2.116)

## B. Conference Publications

*Total of 29 Conference Proceedings Publications*

**i. Technical Manuscripts:**

22. M. Hossain, A. Tatulian, H. Reddy Thummala, R. F. DeMara, and **S. Salehi**, "Low Energy and Area Efficient ANN-based Digit Recognition using Spin-based Progressive Modular Redundancy," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS'23)*, Monetary, CA, May 21-25, 2023.

21. C. Bandi, R. Hassan, S. Golchin, M. Tsai, S. Manoj P. D., S. Rafatirad, and **S. Salehi**, "Automated Supervised Topic Modeling Framework for Hardware Weaknesses," in *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED'23)*, San Francisco, CA, USA, April 5-7, 2023.

20. K. Immanuel Gubbi, T. Sheaves, **S. Salehi**, S. Manoj P. D., S. Rafatirad, A. Sasan, and H. Homayoun, "Survey of Machine Learning for Electronic Design Automation," in *Proceedings of ACM Great Lake Symposium on VLSI (GLSVLSI'22)*, Orange County, CA, June 6-8, 2022.

19. **S. Salehi**, T. Sheaves, K. Immanuel Gubbi, S. A. Beheshti-Shirazi, S. Manoj P. D., S. Rafatirad, A. Sasan, T. Mohsenin, and H. Homayoun, "Neuromorphic-Enabled Security for IoT," in *Proceedings of IEEE International New Circuits and Systems Conference (NEWCAS'22)*, Quebec, Canada, June 19-22, 2022.

18. G. Kolhe, T. Sheaves, K. Immanuel Gubbi, **S. Salehi**, S. Manoj P. D., S. Rafatirad, A. Sasan, and H. Homayoun, "LOCK & ROLL: Deep-Learning Power Side-Channel Attack Mitigation using Emerging Reconfigurable Devices and Logic Locking," in *Proceedings of ACM Design Automation Conference (DAC'22)*, San Francisco, CA, July 10-14, 2022.

17. R. Tsang, D. Joseph, A. Asmita, **S. Salehi**, N. Carreon, P. Mohapatra, and H. Homayoun, "FANDEMIC: Firmware Attack Construction and Deployment on Power Management Integrated Circuit and Impacts on IoT Applications," in *Proceedings of Network and Distributed System Security Symposium (NDSS)*, San Diego, CA, February 27-March 3, 2022.

16. G. Kolhe, **S. Salehi**, T. Sheaves, S. Manoj P. D., S. Rafatirad, A. Sasan, and H. Homayoun, "Securing Hardware via Dynamic Obfuscation Utilizing Reconfigurable Interconnect and Logic Blocks," in *Proceedings of ACM Design Automation Conference (DAC'21)*, San Francisco, CA, USA, December 5-9, 2021.

15. M. Hossain, **S. Salehi**, D. Mulvaney, and R. F. DeMara, "Embedded STT-MRAM Energy Analysis for Intermittent Applications Using Mean Standby Duration," in *Proceedings of IEEE International Conference on Electronics, Circuits and Systems (ICECS'21)*, Dubai, UAE, November 28-December 1, 2021.

14. H. Wang, **S. Salehi**, H. Sayadi, A. Sasan, T. Mohsenin, S. Manoj P. D., S. Rafatirad, and H. Homayoun, "Evaluation of Machine Learning-based Detection against Side-Channel Attacks on Autonomous Vehicle," in *Proceedings of IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS'21)*, Virtual, June 6-9, 2021.

13. C. Bandi, **S. Salehi**, R. Hassan, S. Manoj P. D., H. Homayoun, and S. Rafatirad, "Ontology-Driven Framework for Trend Analysis of Vulnerabilities and Impacts in IoT Hardware," in *Proceedings of IEEE International Conference on Semantic Computing (ICSC'21)*, Laguna Hills, CA, USA, Virtual, January 27-29, 2021.

12. A. Tatulian, **S. Salehi**, and R. F. DeMara, "Mixed-Signal Spin/Charge Reconfigurable Array for Energy-Aware Compressive Signal Processing," in *Proceedings of IEEE International Conference on Reconfigurable Computing and FPGAs (ReConfig'19)*, Cancun, Mexico, December 9-11, 2019.

11. G. Camero, **S. Salehi**, and R. F. DeMara, "A Spin-based Analog to Digital Converter Interactive Simulation Framework," in *Proceedings of IEEE International Conference on Reconfigurable Computing and FPGAs (ReConfig'19)*, Cancun, Mexico, December 9-11, 2019.

10. S. Sheikhfaal, S. D. Pyle, **S. Salehi**, and R. F. DeMara, "An Ultra-Low Power Spintronic Stochastic Spiking Neuron with Self-Adaptive Discrete Sampling," in *Proceedings of IEEE International Midwest Symposium on Circuits and Systems (MWSCAS'19)*, Dallas, TX, USA, August 4-7, 2019.

9. **S. Salehi**, A. Zaeemzadeh, A. Tatulian, N. Rahnavard, and R. F. DeMara, "MRAM-based Stochastic Oscillators for Adaptive Non-Uniform Sampling of Sparse Signals in IoT Applications," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI'19)*, Miami, FL, USA, July 15-17, 2019.

8. **S. Salehi**, R. Zand, A. Zaeemzadeh, N. Rahnavard, and R. F. DeMara, "AQuRate: MRAM-based Stochastic Oscillator for Adaptive Quantization Rate Sampling of Sparse Signals," in *Proceedings of ACM Great Lake Symposium on VLSI (GLSVLSI'19)*, Tysons Corner, VA, USA, May 9-11, 2019.
**Best Poster of the Conference Award Winner**

7. **S. Salehi**, R. Zand, and R. F. DeMara, "Clockless Spin-based Look-Up Tables with Wide Read Margin," in *Proceedings of ACM Great Lake Symposium on VLSI (GLSVLSI'19)*, Tysons Corner, VA, USA, May 9-11, 2019.

6. **S. Salehi**, and R. F. DeMara, "BGIM: Bit-Grained Instant-on Memory Cell for Sleep Power Critical Mobile Applications," in *Proceedings of IEEE International Conference on Computer Design (ICCD'18)*, Orlando, FL, USA, October 7-10, 2018.

5. **S. Salehi**, and R. F. DeMara, "Process Variation Immune and Energy Aware Sense Amplifiers for Resistive Non-Volatile Memories," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS'17)*, Baltimore, MD, USA, May 28-31, 2017.

4. N. Khoshavi, **S. Salehi**, and R. F. DeMara, "Variation-Immune Resistive Non-Volatile Memory using Self-Organized Sub-Bank Circuit Designs," in *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED'17)*, Santa Clara, CA, USA, March 13-15, 2017.
**Best Paper of the Session and Best Paper of The Conference Award Nominee - Top 10%**

3. **S. Salehi**, and R. F. DeMara, "Energy and Area Analysis of a Floating-Point Unit in 15nm CMOS Process Technology," in *Proceedings of IEEE SoutheastCon (SECon'15)*, Fort Lauderdale, FL, USA, April 9-12, 2015.

2. R. A. Ashraf, A. Al-Zahrani, N. Khoshavi, R. Zand, **S. Salehi**, A. Roohi, M. Lin, and R. F. DeMara, "Reactive Rejuvenation of CMOS Logic Paths using Self-Activating Voltage Domains," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS'15)*, Lisbon, Portugal, May 24-27, 2015.

1. P. Soleiman, **S. Salehi**, M. Mahmoudi, M. Ghavami, H. Moradi, and H. Pouretemad, "RoboParrot: A Robotic Platform for Human Robot Interaction, Case of Autistic Children," in *Proceedings of IEEE International Conference on Robotics and Mechatronics (ICRoM'14)*, Tehran, Iran, October 15-17, 2014.

**ii. STEM Educational Manuscripts:**

7. G. Camero, **S. Salehi**, and R. F. DeMara, "Adaptive Behavioral Simulation Framework for 2-Terminal MTJ-based Analog to Digital Converter," in *Proceedings of IEEE Integrated STEM Education Conference (ISEC'20)*, Princeton, New Jersey, March 28, 2020.

6. **S. Salehi**, and R. F. DeMara, "Virtualized Active Learning for Undergraduate Engineering Disciplines (VALUED): A Pilot in a Large Enrollment Classroom," in *Proceedings of IEEE Frontiers in Education Conference (FIE'19)*, Cincinnati, Ohio, October 16-19, 2019.

5. **S. Salehi**, R. Zand, and R. F. DeMara, "Learner Capstone Panels for Immersing Undergraduates in Mechanisms of Engineering Research," in *Proceedings of American Society of Engineering Education National Annual Conference (ASEE'19)*, Tampa Bay, Florida, June 15-19, 2019.

4. R. F. DeMara, **S. Salehi**, and N. Khoshavi, S. Pyle, "Scalable Delivery and Remediation of Engineering Assessments using Computer-Based Assessment," in *Proceedings of IEEE Integrated STEM Education Conference (ISEC'19)*, Princeton, New Jersey, March 16, 2019.

3. R. F. DeMara, **S. Salehi**, B. Chen, and R. Hartshorne, "GLASS: Group Learning At Significant Scale via wifi-Enabled Learner Design Teams in an ECE Flipped Classroom," in *Proceedings of American Society of Engineering Education National Annual Conference (ASEE'17)*, Columbus, Ohio, June 25-28, 2017.

2. R. F. DeMara, **S. Salehi**, and S. Muttineni, "Exam Preparation through Directed Video Blogging and Electronically-Mediated Realtime Classroom Interaction," in *Proceedings of American Society of Engineering Education Southeast Section Conference (ASEE-SE'16)*, Tuscaloosa, Alabama, USA, March 13-15, 2016.

1. R. F. DeMara, **S. Salehi**, N. Khoshavi, R. Hartshorne, and B. Chen, "Strengthening STEM Laboratory Assessment Using Student-Narrative Portfolios Interwoven with Online Evaluation," in *Proceedings of American Society of Engineering Education Southeast Section Conference (ASEE-SE'16)*, Tuscaloosa, Alabama, USA, March 13-15, 2016.

## V. Selected Funding Proposal Development

**University of Arizona, International Research Grant** **Co-Principal Investigator (Co-PI)**
*Award Amount: $48,357.00* *End Date: December 31, 2023*
Co-composed the proposal titled "Collaboratory for AI-enabled Resilient Smart Cyber-Physical Systems AI-RSCPS"

**NSF, CISE/CCF, CRA-CCC** **Principal Investigator (PI)**
*Award Amount: $254,034.00, Award Number: 2030859/CIF2020-UCD-50* *End Date: August 31, 2022*
Composed the proposal titled "SHIELD: Secure Hardware for IoT using Emerging-devices against side-channeL Deep-learning attacks"

**NSF, IUCRC CHEST** **Co-Principal Investigator (Co-PI)**
*Award Amount: $75,000.00* *End Date: August 31, 2022*
Co-composed the proposal titled "SHERLOCK: Power Side Channel Attack-Resilient Hardware using Emerging Reconfigurable Devices and Logic Locking"

**NSF, IUCRC CHEST** **Assisted Through Award of Funding**
*Award Amount: $75,000.00* *End Date: August 31, 2022*
Co-Composed the proposal titled "Do you Trust Your Standard Cell Library: Trojan Resilience Untrusted Cell Library Analysis, Detection, and Mitigation"

**NSF, SaTC** **Assisted Through Award of Funding**
*Award Amount: $1,200,000.00, Award Number: 2155029 & 2155002* *End Date: June 30, 2026*
Co-composed the proposal titled "Targeted Microarchitectural Attacks and Defenses in Cloud Infrastructure"

**UC Davis, 2021 Dean's Collaborative Research award (DECOR)** **Assisted Through Award of Funding**
*Award Amount: $60,000.00* *End Date: June 30, 2022*
Co-Composed the proposal titled "UC Davis Institute for Hardware and AI-enabled Cyber Security"

**UC Noyce Initiative** **Assisted Through Award of Funding**
*Award Amount: $225,000.00* *End Date: August 31, 2022*
Co-Composed the proposal titled "Cross-Layer Approach to Enhance Security/Privacy of AI-enabled IoT Eco-Systems"

**UC Noyce Initiative** **Assisted Through Award of Funding**
*Award Amount: $200,000.00* *End Date: August 31, 2022*
Co-Composed the proposal titled "Firmware and Hardware Trojan Vulnerability Detection and Mitigation in IoT Supply-Chain"

**NSF, ECCS, CCSS** **Assisted Through Award of Funding**
*Award Amount: $441,711.00, Award Number: 1810256* *End Date: August 31, 2021*
Co-composed the proposal titled "Cross-layer Adaptive Rate/Resolution Design for Energy-Aware Acquisition of Spectrally Sparse Signals Leveraging Spin-based Devices"

**NSF, CISE/CCF, SHF-Small**: Co-composed the proposal titled "Heterogeneous Technology Fabrics for Next Generation Reconfigurable Computing"

**SRC, HWS**: Co-composed the white paper titled "Hardware Trojan Detection utilizing Intelligent Adaptive Compressive Sensing"

**SRC, AMS-CSD**: Co-composed the white paper titled "Mixed-Signal Reconfigurable Array for Energy-Aware Neuromorphic Processing"

**NSF, CISE/EHR, EXP**: Co-composed the proposal titled "SAPPHIRE: Mining of Computerized Formative Assessments to Automatically Generate Personalized Laboratory Experiences"

**NSF, IUSE/EHR, EXP**: Co-composed the proposal titled "BLUESHIFT: Rebalancing Engineering Engagement, Integrity, and Learning Outcomes across an Electronically-Enabled Remediation Hierarchy"

# VI. Honors and Awards

## A. Awards and Scholarships

*Total of 11 Scholastic Recognitions providing $8,850 (cumulative).*

- University Award for Excellence by a Graduate Teaching Assistant at the University of Central Florida, Spring 2016.

*Monetary Amount:* ***$1,000***

**Description:** Graduate Teaching Assistants (GTAs) who are nominated from all course Instructors among all of the degree programs across all of the colleges at the University of Central Florida compete for this prestigious award. Excellence in serving as a Graduate Teaching Assistant is demonstrated by evidences such Instructor evaluations, student letters attesting to teaching excellence, lab syllabi and materials created, a sample projects, and instructional innovations developed, introduced, evaluated, and/or published. During each calendar year, a single GTA is selected by Deans and faculty representatives for this recognition of teaching excellence, instructional innovation, and future faculty potential.

- Award for Excellence by a Graduate Teaching Assistant at the College of Engineering and Computer Science of the University of Central Florida, Spring 2016.

*Monetary Amount:* ***$500***

- Award for Excellence by a Graduate Teaching Assistant at the Department of Electrical and Computer Engineering of the University of Central Florida, Spring 2016.
- Best Presentation of the Symposium Award Winner at the University of California Davis Postdoctoral Research Symposium 2021 (PRS-2021), March 31, 2021.

*Monetary Amount:* ***$250***

- Best Poster of the Conference Award Winner at the ACM Great Lake Symposium on VLSI (GLSVLSI'19), May 9-11, 2019.
- Best Student Poster and Second Best Poster Presentation at the Digitally-Mediated Team Learning (DMTL) National Science Foundation (NSF)-Sponsored Workshop, March 31, 2019.

*Monetary Amount:* ***$100***

- Best Paper of the Session and Best Paper of The Conference Award Nominee at the IEEE International Symposium on Quality Electronic Design (ISQED'17), March 13-15, 2017.
- Frank Hubbard Engineering Endowed Scholarship for the 2019-2020 academic year.

*Monetary Amount:* ***$1,000***

- David T. and Jane M. Donaldson Memorial Graduate Scholarship for the 2018-2019 academic year.

*Monetary Amount:* ***$5,000***

- Daniel D. Hammond Engineering Graduate Scholarship for the 2017-2018 academic year.

*Monetary Amount:* ***$1,000***

- Nominated for the "30-Under-30" Award at the University of Central Florida, Fall 2019.
- Nominated for the Postdoctoral Research Excellence Award at the University of California Davis, Spring 2022

### B. Orchestration of Presentation and Travel Grants

*Total of 6 Research and Travel Grants providing $19,950 (cumulative).*

- National Science Foundation (NSF) Student Travel Grant to attend the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2019.

*Monetary Amount:* ***$500***

- National Science Foundation (NSF) Student Travel Grant to attend the IEEE International Conference on Computer Design (ICCD), 2018.

*Monetary Amount:* ***$750***

- Student Travel Grant to attend the Design Automation Conference (DAC) Ph.D. Forum, 2019.

*Monetary Amount:* ***$700***

- University of Central Florida Student Government Association Registered Student Organization Conference Participation Grant, 2017, 2018, and 2019.

*Monetary Amount:* ***$14,000***

- University of Central Florida College of Graduate Studies Conference Presentation Grant, 2015, 2016, 2017, and 2019.

*Monetary Amount:* ***$2,000***

- University of Central Florida Student Government Association Individual Conference Presentation Grant, 2015, 2016, 2017, 2019.

*Monetary Amount:* ***$2,000***

## C. Technical Paper Reviewer/Referee

- Refereed Paper for *IEEE Transactions on Very Large Integrated Systems (TVLSI)*, Reviewer of Record, 2018, 2019, 2021, and 2023.
- Refereed Paper for *IEEE Transactions on Computer-Aided Design (TCAD)*, Reviewer of Record, 2019, 2021, 2022, and 2023.
- Refereed Paper for *IEEE Transactions on Computers (TC)*, Reviewer of Record, 2015, 2018, 2022, and 2023.
- Refereed Paper for *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, Reviewer of Record, 2016, 2020, and 2021.
- Refereed Paper for *IEEE Journal of Solid-State Circuits (JSSC)*, Reviewer of Record, 2021.
- Refereed Paper for *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Reviewer of Record, 2021.
- Refereed Paper for *IEEE Transactions on Nanotechnology (TNANO)*, Reviewer of Record, 2020.
- Refereed Paper for *ACM Journal of Emerging Technologies in Computing Systems (JETC)*, Reviewer of Record, 2020.
- Refereed Paper for *IEEE Access*, Reviewer of Record, 2018 and 2020.
- Refereed Paper for *IEEE Open Journal of Circuits and Systems (OJCAS)*, Reviewer of Record, 2020.
- Refereed Paper for *IEEE Transactions on Emerging Topics in Computing (TETC)*, Reviewer of Record, 2019.
- Refereed Paper for *International Journal of Electrical Engineering Education (IJEEE)*, Reviewer of Record, 2018.
- Refereed Paper for *IEEE International Symposium on Quality Electronic Design (ISQED)*, Reviewer of Record, 2022.
- Refereed Paper for *ACM Great Lake Symposium on VLSI (GLSVLSI)*, Reviewer of Record, 2020 and 2021.
- Refereed Paper for *IEEE/ACM Design Automation Conference (DAC)*, Reviewer of Record, 2021, 2022, and 2023.
- Refereed Paper for *IEEE International Conference on VLSI Design (VLSID)*, Reviewer of Record, 2022.
- Refereed Paper for *American Society of Engineering Education (ASEE)*, Reviewer of Record, 2016, 2017, 2018, and 2019.
- Refereed Paper for *IEEE Frontiers In Education (FIE)*, Reviewer of Record, 2019.
- Refereed Paper for *IEEE SoutheastCon*, Reviewer of Record, 2018.
- Refereed Paper for *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2021.

- Refereed Paper for *IEEE/ACM International Conference On Computer-Aided Design (ICCAD)*, 2020, 2021.
- Refereed Paper for *Network and Distributed Systems Security Symposium (NDSS)*, 2021.
- Refereed Paper for *IEEE Computer Society Annual International Symposium on VLSI (ISVLSI)*, 2015, 2016, 2017, and 2018.

### D. Professional Service and Activities

- *Institute of Electrical and Electronics Engineers (IEEE)*, Student Member 2015-2020, Member since 2020.
- *American Society of Engineering Education (ASEE)*, Member since 2018.
- Invited to serve as the Graduate Student at Large to the *Activity and Service Fee (A&SF) Budget Committee* of the University of Central Florida, Fall 2016.
- Founding President of *Student Laureates of STEM Teaching and Learning (SLSTL)* Registered Student Organization at the University of Central Florida, Summer 2016-Spring 2020.
- Founding President of *Computer Hardware Innovation and Design Association (CHIDA)* Registered Student Organization at the University of Central Florida, Spring 2019-Spring 2020.
- Invited to serve as the Student Representative to the *Teaching Incentive Program (TIP) Faculty Award Committee* of the College of Engineering and Computer Science (CECS), Spring 2016.
- Elected to be the Chairman of *Conference Registration and Travel (CRT) Committee* at the Student Government Association Senate of the University of Central Florida, Spring 2016-Fall 2016.
- Elected to be a Member of *Conference Registration and Travel (CRT) Committee* at the Student Government Association Senate of the University of Central Florida, Fall 2015-Fall 2016.
- Elected as a Senator at *Student Government Association (SGA) Senate* of the University of Central Florida, Fall 2015-Fall 2016.
- Conference Volunteer for *IEEE International Symposium Series on Computational Intelligence (ISSCI)*, Orlando, FL, Fall 2014.

## VII. Conference and Workshop Organization and Delivery

- Organizing Committee Member at *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Knoxville, Tennessee, June 5-7, 2023.
- Technical Program Committee (TPC) Member at *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, California, July 9-13, 2023.
- Technical Program Committee (TPC) Member at *IEEE International Symposium on Quality Electronic Design (ISQED)*, San Francisco, California, April 5-7, 2023.
- Technical Program Committee (TPC) Member at *IEEE International Conference on VLSI Design (VLSID)*, Hyderabad, India, January 8-12, 2023.
- Co-Organizer, Co-Creator, and Instructor of "ML-Assisted Hardware Trojan Detection" Education Class at *IEEE/ACM Embedded Systems Week (ESWEEK)*, Shanghai, China and Phoenix, Arizona (Virtual), October 7-14, 2022.

- Chair of a Session at *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, CA, July 10-14, 2022.
- Chair of a Session at *IEEE International Symposium on Quality Electronic Design (ISQED)*, Virtual, April 6-7, 2022.
- Technical Program Committee (TPC) Member at *IEEE/ACM Design Automation Conference (DAC)*, San Francisco, California, July 10-14, 2022.
- Technical Program Committee (TPC) Member at *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Durham, North Carolina, June 22-25, 2021.
- Chair of a Session at *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Durham, North Carolina, June 22-25, 2021.
- Chair of a Poster Session at *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Beijing, China, September 8-11, 2020.
- Co-Organizer, Co-Creator, and Instructor of "Virtualized Active Learning in STEM" Pre-Conference Workshop at *IEEE Frontiers In Education (FIE)*, Cincinnati, Ohio, October 16-19, 2019.
  - Workshop with 21 participants from universities across the world
  - Co-created 6 online modules in Canvas for Teachers
  - 100% respondents agreed workshop motivated them to use technology-enhanced learning in their courses
- Co-Organizer, Co-Creator, and Panel Moderator of "In-Memory Processing for Future Electronics" Panel at *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Washington, D.C., USA, May 9-11, 2019.
  - Innovated interactive web-based approach for audience participation in panel discussion
  - Transportable to other technical conference venues and lecture formats
- Round Table Participant at the *NSF-sponsored workshop University-Industry Partnerships and The Future of Work at the Human-Technology Frontier*, Orlando, FL, September 24, 2019.
- Panelist, *Digitizing and Remediating STEM Assessments Panel*, University of Central Florida, Orlando, FL, 2016-2018.

## VIII. Presentation in Conferences/Seminars/Symposiums

- PowerPoint presentation at *IEEE NEWCAS*, Quebec City, Quebec, Canada, June 19-22, 2022.
- Poster presentation at *30th NITRD Symposium*, Washington, D.C., USA, May 25, 2022.
- Poster presentation at *CRA/CCC CIFellows Cohort Building Event*, Washington, D.C., USA, May 26, 2022.
- PowerPoint presentation at *the University of California Davis Postdoctoral Research Symposium 2021*, Davis, California, USA, Virtual, March 31, 2021. **Best Presentation of the Symposium Award Winner.**
- PowerPoint presentation at *IEEE ICSC*, Laguna Hills, California, USA, January 27-29, 2021.
- PowerPoint presentation at *IEEE ISEC*, Princeton, New Jersey, USA, Virtual, March 28, 2020.
- Poster presentation at *IEEE FIE*, Cincinnati, Ohio, USA, October 16-19, 2019.
- PowerPoint presentation at *IEEE MWSCAS*, Dallas, Texas, USA, August 4-7, 2019.
- PowerPoint presentation at *IEEE ISVLSI*, Miami, Florida, USA, July 15-17, 2019.

- PowerPoint presentation at *ASEE National*, Tampa, FL, June 15-19, USA, 2019.
- Poster presentation at *ACM DAC Ph.D. Forum*, Las Vegas, Nevada, USA, June 3-6, 2019.
- Poster presentation at *ACM GLSVLSI*, Tysons Corner, Virginia, USA, May 9-11, 2019. **Best Poster of Conference Award Winner.**
- Poster presentation at *Digitally-Mediated Team Learning (DMTL) NSF-Sponsored Workshop*, *"LMS-Integrated Digitally-Mediated Team Learning Toolset,"* Orlando, Florida, USA, March 31-April 2, 2019. **Best Student Poster of the Workshop Award Winner.**
- PowerPoint presentation at *IEEE ICCD*, Orlando, Florida, USA, October 7-10, 2018.
- PowerPoint presentation at *ASEE National*, Salt Lake City, Utah, USA, June 24-27, 2018.
- PowerPoint presentation at *ASEE National*, Columbus, Ohio, USA, June 25-28, 2017.
- Poster presentation at *IEEE ISCAS*, Baltimore, Maryland, USA, May 28-31, 2017.
- PowerPoint presentation at *ASEE Southeastern*, Tuscaloosa, Alabama, USA, March 13-15, 2016.
- PowerPoint presentation at *IEEE SoutheastCon*, Fort Lauderdale, Florida, USA, April 9-12, 2015.
- Invited Seminar Talk on Distributed Computing, "Models of Computation and Computational Models Seminar," *ACM Student Chapter*, University of Tehran, Tehran, Iran, 2012.

## X. Internships and Industry Experience

**Summer Intern** **May 2012-August 2012**
*Iranian Embedded Systems* *Tehran, Iran*

- Study of *Texas Instruments Wireless Sensor Networks*
- Design and implementation of an Application Specific Wireless Sensor Network using *Texas Instruments CC2431*
  - Design and implementation of a Graphical User Interface (GUI) for the designed device
- Design and implementation of interfacing embedded systems and Printed Circuit Boards (PCBs) for *Xilinx Virtex5* and *Xilinx Spartan3* FPGAs
- Design and implementation of an Educational General Purpose Board for the University of Tehran's Computer Lab
  - Design and implementation of a Graphical User Interface (GUI) for the designed board

**Technician** **2010-2013**
*Persian Tronix Co., Tehran, Iran*
Advanced laptop repairing and troubleshooting of both hardware and software

**PCB Designer** **2010-2014**
*University of Tehran, Tehran, Iran*
Designing Printed Circuit Boards (PCBs) for variety of purposes as a freelance work at the University of Tehran