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Embedded STT-MRAM Energy Analysis for Intermittent Applications using Mean Standby Duration

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***Abstract*—Power, area, and delay trade-offs occupy a vital role in early pre-fabrication design decisions for various System-on-Chip (SoC) and intermittently powered devices. The approach taken herein is to explicitly incorporate device technology trade-offs during the initial circuit design process. Specifically, the asymmetry between read/write energy consumption and active/standby duty cycles are used to facilitate trade-offs between use of embedded 6-Transistor Static Random Access Memory cell (6T-SRAM) versus embedded Magnetic Random-Access Memory (MRAM)-based on Spin Torque Transfer Magnetic Tunnel Junction (STT-MTJ) single bit cell structure of two transistors and one MTJ (2T-1R). A model is developed and validated to estimate power in hybrid Complementary Metal Oxide Semiconductor (CMOS)/MTJ technology with coefficient of determination R^2>0.95. The approach employs three new metrics: *Mean Standby Duration (MSD)*, *Mean Active Duration (MAD)*, and *Power Dissipation Scaling Ratio (PDSR)*. Thresholds of MSD>0.995 and MAD<0.005 were determined to be inflection points for lifetime energy justification for considering MTJ devices in terms of total power. Results substantiate a transportable approach for the inclusion of emerging logic devices by considering the energy profile of some intermittently powered applications by parameterizing the workload using the metrics defined herein.**

Keywords— Leakage Power, Power Dissipation Scaling Ratio (PDSR), Spin-based devices, Technology Scaling, Embedded MRAM

I. INTRODUCTION

As current trends in scalable technologies advance, the role of leakage power becomes increasingly prominent. Until recently, feature size and supply voltage of the scaled technologies have followed Dennard scaling, which such trend has diverged for deep sub-micron technologies. Scaled devices portrayed using Predictive Technology Model (PTM) [1] simulation may diverge by one to two orders of magnitude [2]. At sub-22nm static power dissipation now accounts for more than 50% of the die-level power dissipation, precipitating a growing challenge for intermittently powered devices with limited power sources [3].

The majority of static power dissipation takes place within embedded Static Random-Access Memory (SRAM) cells. While SRAM cells can be expected to draw a considerable standby current to retain data, Magnetic Tunnel Junction (MTJ) devices dissipate near-zero standby power. Thus, Magnetic Random-Access Memory (MRAM) cells based on MTJ devices offer a viable alternative to CMOS-based memory cells while imparting area-efficiency, low read access time, and backend compatibility with existing CMOS fabrication processes. Although the effects of technology scaling have been studied for CMOS devices, similar studies including concrete comparisons to emerging MTJ devices can offer valuable insights to optimize a circuit's lifetime energy consumption and maintain its energy budget.

To extend beyond recent efforts for modeling of 6-Transistor SRAM (6T-SRAM) cells, herein we consider technology scaling trends of Spin Torque Transfer Magnetic Random-Access Memory (STT-MRAM) with respect to power dissipation and area, including the impact of Process Variation (PV) [4]. These effects are incorporated herein into models utilized via SPICE simulation along with Predictive Technology Model (PTM) libraries [1] to ascertain MRAM vs. SRAM technology inflection trade-off points. Quantitative results obtained also refine lifetime energy estimates over the operational lifetime which are parameterized in terms of three new metrics: Mean Standby Duration (MSD), Mean Active Duration (MAD), and Power Dissipation Scaling Ratio (PDSR) defined in Section IV.

The contributions of this paper include:

- An analytical model of the scaling effects for SRAM vs STT-MRAM in terms of static and write power dissipation for sub-micron technology nodes, in presence of PV.
- Workload-driven parameters of components' MSD and MAD, which are used to ascertain their duty cycle impacts on total power dissipation of candidate memory cell designs.
- A new metric, PDSR, which extends technology scaling to embedded MRAM devices.
- Quantification of static and dynamic power dissipation in bit-cell 6T-SRAM and 2T-1R MRAM cell based on MSD, MAD, and PDSR.

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II. BACKGROUND

First, we contrast qualitatively the power profiles of SRAM and MRAM technologies for embedded intermittently powered devices. The static power dissipation can be modeled by taking into account underlying mechanism such as gate tunneling and conduction through reverse-biased p-n junctions, as certain non-idealities stemming from the subthreshold leakage current result from their CMOS transistors [5]. Additionally, dynamic power dissipation is a result of write operation of the memory cell. Moreover, the reliability of write operations are directly related to the device characteristics. For SRAM, write reliability might not be of much importance since the overhead cost of an additional write operation in terms of delay and power dissipation is negligible. However, using MTJ devices, overhead cost of an additional write operation would be significant and it can become a burden on the dynamic power dissipation, and some manufacturers conduct two write cycles [6]. MTJ characteristics outline the MRAM's reliability in terms of write failures and read disturb failures, which mainly arise due to thermal instability of the MTJ nanomagnet, insufficient switching duration, readability degradation due to technology scaling on the access transistor of the MTJ device, and write polarization asymmetry while switching between '0' and '1' states of the MTJ [7].

The primary contributor to leakage power dissipation in CMOS transistors is the subthreshold leakage that is caused by the current that flows from drain to source when the transistor is in standby mode. The leakage current (I_{lkg}) can be modeled by (1) as given in [8]:

$$I_{lkg} = I_{S0} \times \left(e^{-V_{off}/nV_t}\right) \times \left(e^{-V_{th}/nV_t}\right) \tag{1}$$

where, *n* is the threshold swing factor, V_{gs} is the transistor gate to source voltage, V_{th} is the threshold voltage, $I_{S0} = W/L \times I_{S0}^{'}$ is the current dependent on the transistor's geometry [8], W and L are the length and width of the transistor channel, $V_t = kT/q$ is the thermal voltage, V_{off} is an empirically determined model parameter, *k* represents the Boltzmann constant, *T* accounts for the external temperature, and *q* is the electron charge. All these parameters are obtainable from the Predictive Technology Model (PTM) libraries as per [9]. The dynamic and static power dissipations of the SRAM cell can be estimated using (2) and (3), respectively as:

$$P_{dynamic} = C_L \times {V_{CC}}^2 \times f_{clk} \tag{2}$$

$$P_{static} = I_{lkg} \times V_{CC} \tag{3}$$

where, C_L is the capacitive load, V_{CC} is the supply voltage, and f_{clk} is the clock frequency. Total power dissipation is determined through the dynamic and static power, with near negligible power contributed from the short circuit current that is hence ignored for our calculations. The leakage current can be modeled based on gate tunneling and conduction through reverse-biased p-n junctions comprising the 6 MOSFET cell as in [5].

According to the 2017 ITRS Magnetism Roadmap, nanomagnetic devices are capable post-CMOS candidates, which include MTJ devices that have been commercialized [10]. STT-MRAM considered herein utilizes MTJ devices comprised of an insulating oxide layer separating two ferro-magnetic layers [11]. One of the layers has a pinned magnetic polarization, which is called the fixed layer, while the magnetic polarization of the other ferro-magnetic layer is free to be changed by various switching mechanisms and is named the free layer. When the polarization of the ferro-magnetic layers is in the same direction, the MTJ device is said to be in the Parallel (P) low resistance state, analogous to Logic '0' condition. When the layers are in the opposite polarization, the MTJ is said to be in Anti-Parallel (AP) state, analogous to Logic '1' condition with high resistance across the device. The most popular MTJ switching mechanism is STT, where data is written into the bit-cell by passing a spin-polarized current through the MTJ device.

Equations (4) and (5) denote STT-MRAM static and dynamic power dissipations respectively, where f_{data} is the data throughput frequency, $I(t)$ represents the write current that passes through the MTJ device and T is the pulse duration for the write operation [12]. Since the MTJ devices have near-zero leakage as discussed earlier, the majority of leakage power dissipation comes from the write transistors where I_{lkg}^{MRAM} is the leakage current through the write transistors in OFF-state of the STT-MRAM cell and V_{CC} is the supply voltage discussed in Section III. These simplified equations are used to provide a model to estimate the power dissipation of STT-MRAM bit-cells.

$$P_{dynamic} = f_{data} \times V_{CC} \times \int_0^T I(t)dt \tag{4}$$

$$P_{static} = I_{lkg}^{MRAM} \times V_{CC} \tag{5}$$

Several models exist for estimating the static and dynamic power scaling trends for SRAM devices and corresponding memory array structures, developed over the past two decades [8], [9], [13]. However, some of those suffer from inaccuracies because node capacitances can be difficult to estimate using simple analytical models. Stillmaker and Baas developed a fast and scalable model for determining the area, power, and delay performances of a CMOS system based on a cascaded chain of inverters [2]. Meanwhile, Togashi designed a 16bit/32bit binary counter using MTJ devices and compared power dissipation with corresponding CMOS based design in [14]. Chun et al. studied the scaling trends of read and write performances of STT-MRAM along with Monte Carlo simulations to consider Process Variation (PV) effects [4]. Furthermore, Jaiswal analyzed scaling trends from 45 nm to 11 nm for various performance parameters for bit-cells of three different MTJ-based design structures [7].

These and other related works concerning STT-MRAM provide relevant insights into scaling effects on write delay, write energy,

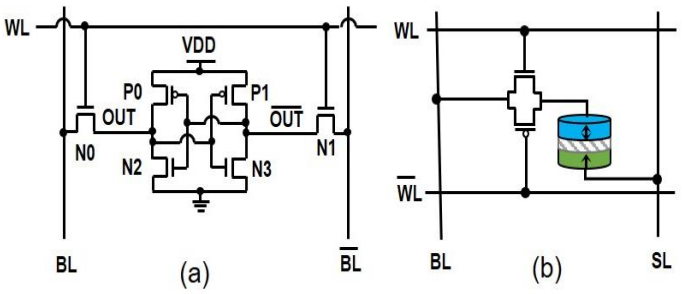

Fig. 1. (a) SRAM bit-cell, (b) STT-MRAM bit-cell addressed herein.

sensing delay and reliability [15], [16]. However, they do not provide a general rule or metric to assist researchers and circuit designers to be able to estimate the power dissipation of hybrid CMOS/MTJ designs at scaled technology nodes. Moreover, previous works do not account for the power efficiency of STT-MRAM memory compared to conventional SRAM memory within intermittently powered processors, where most of the time the system is in standby mode and leakage power dissipation is dominant. Thus, there is a need for a model that considers the time that the memory spends in standby mode compared to that spent in reading from or writing to the memory. Herein, we analyze a 6T-SRAM bit-cell and compare it to a STT-MRAM bit-cell to derive static and dynamic power dissipation trends with regards to trending sub-micron technology nodes ranging from 45 nm to 16 nm. Extending beyond previous works in the related field, in Section IV we also introduce a new metric for power dissipation efficiency estimation comparison in different technology nodes, as well as two new performance parameters called Mean Standby Duration (MSD) and Mean Active Duration (MAD), which are significant considerations within intermittently powered processors using emerging non-volatile devices.

III. Experimental Setup and Approach

The motivation for this paper is to quantify trends in power efficiency achievable using STT-MRAM memory bit-cell versus SRAM down to 16 nm technology nodes. Considering array structure implementations of SRAM and STT-MRAM since the

TABLE I. Technology Parameters for SRAM and MRAM bit-cells

	Parameter		Mean Value and Description			
			45nm	**32nm**	**22nm**	**16nm**
SRAM	**PMOS**	W/L [10]	270/45 nm	192/32 nm	132/22 nm	96/16 nm
	NMOS	W/L [10]	180/45 nm	128/32 nm	88/22 nm	64/16 nm
		W/L [10] Access Transistor	90/45 nm	64/32 nm	44/22 nm	32/16 nm
STT-MRAM	**PMOS**	W/L [10]	90/45 nm	64/32 nm	44/22 nm	32/16 nm
	NMOS	W/L [10]	45/45 nm	32/32 nm	22/22 nm	16/16 nm
	MTJ	Tox [20]	Oxide Thickness			1.5 nm
		Ms0 [20]	Saturation Magnetizaion			456 $A.m^{-1}$
		P_0	Polarization Factor			0.69
		T	Temperature			298 K
		t_c	Critical Thickness			1.5 nm
		TMR [17]	Tunnel Magnetoresistance			120%
		α [11]	Damping Factor			0.007

K= Kelvin, m = meter, A = ampere, nm = 10^-9 meters. W/L = Width/Length ratio of transistor.

TABLE II. STATIC AND DYNAMIC POWER DISSIPATION FOR ISO-WRITE DURATION

Technology Node	STT-MRAM			SRAM		
	Dynamic Power (nW)	Static Power (pW)	Total Power (nW)	Dynamic Power (nW)	Static Power (pW)	Total Power (nW)
45 nm	46286.3	2.2975	46286	171.628	21377.3	193.01
32 nm	30007.8	1.6289	30007	106.604	29541.5	136.14
22 nm	19068.2	1.2880	19068	63.9465	53366.8	117.31
16 nm	12758	0.9869	12758	36.4842	120950	157.43

nW =10^-9 Watts, pW=10^-12 Watts, nm = 10^-9 meters.

peripheral circuitry can vary depending on different implementations, we focus on a single memory bit-cell comparison. Fig. 1(a) depicts a 6-T SRAM memory cell and Fig. 1(b) illustrates an STT-MRAM memory cell consisting of an MTJ device and a transmission gate as the write circuit. The 2T-1R structure is chosen as it is demonstrated to be the optimal configuration to achieve low write energy and low overall power consumption [17]. We utilized PTM [1] for the NMOS and PMOS transistors in both SRAM and STT-MRAM bit-cells, and MTJ device models provided in [18]. We used SPICE for circuit simulations using the parameters listed in Table I or otherwise typical of two-terminal STT-MTJ in the literature [14], [19]. The SRAM transistor parameters are defined to achieve reliable and stable SRAM operation [21], which have shown to be feasible for fabrication as discussed in [10]. All simulations are carried out at temperature T=298 K, with iso-write time of 5 ns for switching operation of both the STT-MRAM and 6T-SRAM bit-cells.

We performed these simulations utilizing four contemporary and trending sub-micron technology nodes, namely 45 nm, 32 nm, 22 nm, and 16 nm with supply voltages (V_{CC}) of 1.0 V, 0.9 V, 0.8 V, and 0.7 V, respectively. Parasitic node capacitance values are important for correct modeling and simulation of memory bit-cells in SPICE. Thus, we further increased the accuracy of our simulation results by accounting for the parasitic node capacitances by designing the layout for the SRAM and STT-MRAM bit-cells and extracting those parasitic capacitances and area from the layout, for the parameters listed in Table I. The MTJ device has a Tunneling Magnetoresistance (TMR) of 120%.

The layout for SRAM and STT-MRAM bit-cells are shown in Fig. 2(a) and 2(b), respectively. According to the layout, the bit-cell area of SRAM and STT-MRAM bit-cells are estimated to be $861F^2$ and $336F^2$, respectively, where F is the feature size or technology node. While this paper examines device technology scaling consideration to evaluate the leakage and dynamic power dissipation, readers interested in detailed post-layout considerations, fabrication aspects, and associated challenges can refer to

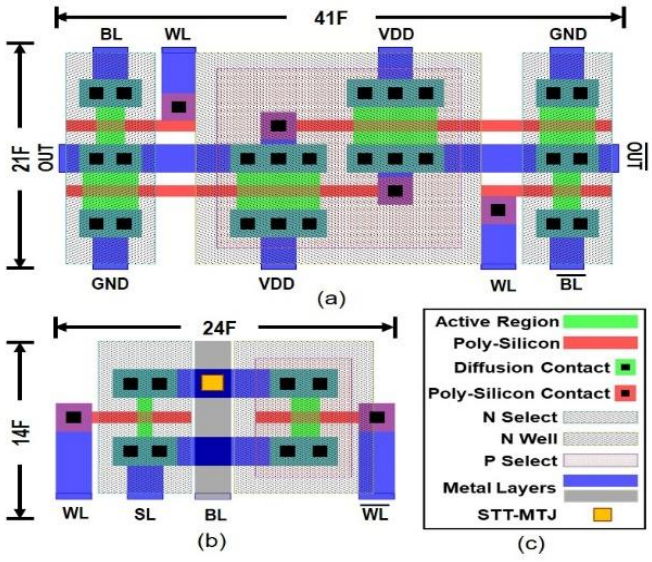

Fig. 2. (a) 6-T SRAM layout, (b) STT-MRAM layout, and (c) legend.

[22][23][24]. Furthermore, the reliability challenges for both SRAM and STT-MRAM bit-cells increase with technology scaling, mainly due to PV effects that result in increased dynamic power dissipation. Thus, we perform 1,000 Monte Carlo (MC) simulation runs considering the variations

discussed to achieve more accurate simulation results in terms of reliability with regards to scaling. For the MC simulations, we have considered 1% variation on the width and length, along with 10% worst case variation on the threshold voltage of NMOS and PMOS transistors. Consideration of 1% variation on the width, length, and thickness of the MTJ free layer as well as 1% variation on the oxide thickness were used [20]. Due to the asymmetric nature of the MTJ write operation, greater write pulse duration is required to switch the MTJ from AP state to P state as compared to switching from P state to AP state. We have considered these variations to account for possible write failures that may occur during the write operation. The parameters of the STT-MRAM bit-cell and the write pulse duration were carefully selected to maintain <0.001 write error rate in the 1,000 MC simulation runs, while achieving a fair comparison with the SRAM bit-cell. Finally, once the simulations are performed, we utilize a polynomial curve fitting using MATLAB on the results to provide a more accurate model for power dissipation of memory bit-cells that can be generalized for scaled technology nodes ranging from 45nm to 16 nm and beyond.

IV. Simulation Results and Discussion

Simulation results for the SRAM and STT-MRAM bit-cell configurations considering iso-write pulse duration of 5ns for all four technology nodes ensures reliable switching of both bit-cells. The power dissipation for both bit-cell configurations are listed in Table II. Additionally, we have plotted the write and static power measurements in logarithmic scale for both SRAM and STT-MRAM power dissipation in different technology nodes for comparison in Fig. 3(a) and 3(b), respectively.

The dynamic power dissipation for both SRAM and STT-MRAM bit-cells are reduced with technology scaling. However, due to the high energy barrier of the MTJ device to maintain increased thermal stability and high endurance, the dynamic power dissipation of STT-MRAM is greater than SRAM. On the other hand, the static power consumption of the SRAM bit-cell increases with technology scaling, which is an expected behavior according to the literature and is mainly caused by short-channel effects and increased leakage current in scaled technology nodes. In contrast, the static power consumption of the STT-MRAM reduces as the technology scales. We conclude from the simulation results that although the static power dissipation of STT-MRAM is significantly smaller than SRAM, the impact of the static power dissipation can be considerably significant in scaled technology nodes. This is because a majority of the lifetime of the memory circuit is spent in standby mode, thus leakage power dissipation becomes a significant contributor to the total power dissipation.

Thus, we introduce two new parameters, namely Mean Active Duration (MAD) and Mean Standby Duration (MSD), to more accurately model power dissipation scenarios for intermittently powered processors. MAD provides a metric for the ratio of the memory time spent performing the write operation, while MSD provides a metric for the ratio of the memory time spent in the standby mode. Considering these two key parameters, we can compare total power dissipation of SRAM and STT-MRAM bit-cells in each technology node using the following metric called Power Dissipation Scaling Ratio (PDSR) described as follows:

$$PDSR = \frac{P_{total_{SRAM}}}{P_{total_{MRAM}}} = \frac{MAD_{SRAM} \times P_{dynamic_{SRAM}} + MSD_{SRAM} \times P_{static_{SRAM}}}{MAD_{MRAM} \times P_{dynamic_{MRAM}} + MSD_{MRAM} \times P_{static_{MRAM}}} \quad (6)$$

Values for MAD and MSD are determined according to the architectural benchmarking for entire memory array and averaged for each bit-cell. By scaling the value of MSD from 0 to 1 in steps of 0.001, and simultaneously varying MAD as (1-MSD), simulations were performed to see the effects of MSD and MAD on PDSR for memory array size of 256x256 bits. Fig. 4 is a logarithmic plot of PDSR vs. MSD, which shows that for MSD > 0.995, i.e., only if memory is in standby mode for more than 0.995 fractions of the mean workload profile time of the intermittently powered device, the performance of MRAM cell in terms of power dissipation becomes better than SRAM cell. For improved readability of the logarithmic plot, only the values of MSD ranging from 0.5 to 1.0 have been shown in the figure, as the effect of MSD on PDSR was not found to be pronounced for MSD <0.5. Note that,

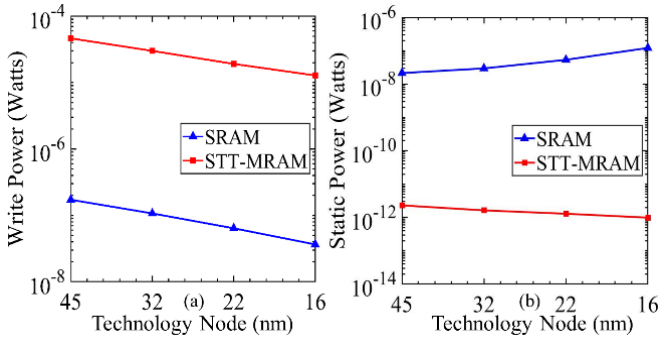

Fig. 3. SRAM vs. STT-MRAM: (a) Dynamic power dissipation, and (b) Static power dissipation.

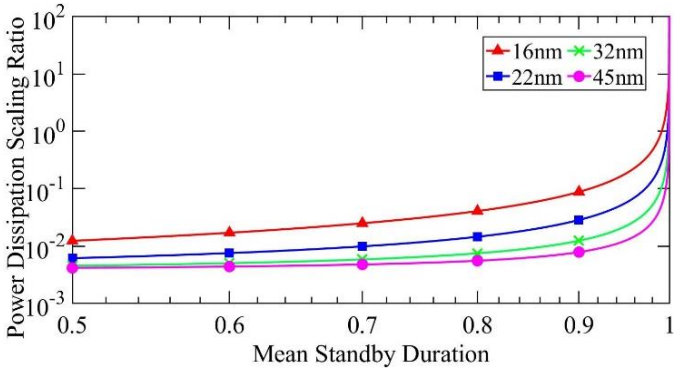

Fig. 4. Power Dissipation Scaling Ratio (PDSR) vs. Mean Standby Duration (MSD) for 16 nm, 22 nm, 32 nm, and 45 nm technology nodes.

embedded MRAM offers a non-volatile memory technology option over Flash memory for intermittently active applications, such as data logging application in sensors for IoT devices [25] and is influenced by the frequency of transition between active and sleep mode. This is because Flash memory has longer write-time, dissipates more power, and has significantly lower write endurance of approximately a thousand write-cycles. MRAM is also a viable alternative to SRAM for ultra-low power IoT devices, which operate at lower frequencies [25]. Table III lists some real-world IoT applications [26], [27] as examples of intermittently active devices that also substantiate MSD metric thresholds mentioned above. Other embedded applications operating under intermittent computational

TABLE III. DUTY CYCLE CALCULATION OF SOME REAL-WORLD IOT APPLICATIONS

IoT Applications	Write Frequency	Embedded Memory	Estimated MSD
Smart Grid [27]	2X hour	Cloud Storage	0.998
Surveillance Camera [26]	1X hour	2GB	0.976
NFC Controllers [26]	1X hour	1280KB	0.999
Key fob [26]	1X minute	4KB	0.999
Thermostat [26]	1X 10 years	512MB	0.999

conditions span FPGA-based [28], long-duration deployment sustainability [29], and high-reliability signal processing systems [30].

For instance, considering the GRID energy dataset, the IoT based smart meter system operates on a 30-minute repetition loop. Considering an operational duration not exceeding 3 seconds per repetition cycle under conditions of maximum memory utilization, a standby duty cycle of 0.9983 is calculated. These results provide valuable insights that the trade-offs between utilizing traditional vs non-volatile memory components in the design depends largely on the workload profiling of intermittently powered applications. Furthermore, once we gathered the SPICE simulation results, we performed a polynomial best curve fitting in MATLAB to obtain predictive models for power dissipation and its scaling trends with a co-efficient of determination, R^2 >0.95, leveraging the methodology proposed in [2]. Table IV lists the polynomial equations for average dynamic and static power dissipations of single SRAM and STT-MRAM bit-cell, where *x* is the target technology node, *p1*, *p2*, and *p3* are coefficients in the equations with values as given in the table, and *nf* is the Normalizing Factor, which is the ratio of target technology node over normalized mean technology node. For example, the static power dissipation for 45nm node STT-MRAM bit-cell with *nf=1.565* was estimated to be 2.44pW using the proposed model, which has an error rate <6% compared to the simulated values provided in Table II.

V. CONCLUSION

As CMOS technologies continue to scale, static power dissipation continues to become a significant design issue constraining intermittently active applications. Results indicate that SRAM bit-cell dynamic power decreases with scaling due to decrease in transistor write current and nominal threshold voltage, whereas static power increases exponentially due to sub-threshold leakage. On the other hand, for an STT-MRAM bit-cell, both static and dynamic power decrease with scaling due to near-zero leakage of the MTJ devices and reduced transistor count compared to 6T-SRAM. These provide utilization trends and limits, quantified using the novel metrics of MAD and MSD, for a more accurate estimation of the power dissipation for SRAM and STT-MRAM comparison in scaled technology nodes the novel metrics of MAD and MSD are used here-in. Namely, it was deduced that when MSD is very high (~0.995), the power dissipation of embedded MRAM attained energy advantages over SRAM. Moreover, further assimilation of transistor-scaling impact with non-volatile devices furthers the understanding of energy profiles for low duty cycle applications.

TABLE IV. PROPOSED POWER DISSIPATION ESTIMATION MODEL

Unit (Watts)	Equation	p1	p2	p3
$\mathbf{P_{st\_SRAM}}$	$nf \times (p1 \times x^{p2})$	5.675×10^{-24}	-2.093	0
$\mathbf{P_{dy\_SRAM}}$	$nf * (p1 \times x^2 + p2 \times x + p3)$	2.771×10^{-9}	5.814×10^{-8}	9.277×10^{-8}
$\mathbf{P_{st\_STT\text{-}MRAM}}$	$nf * (p1 \times x^2 + p2 \times x + p3)$	4.257×10^{-14}	5.483×10^{-13}	1.52×10^{-12}
$\mathbf{P_{dy\_STT\text{-}MRAM}}$	$nf * (p1 \times x^2 + p2 \times x + p3)$	9.398×10^{-7}	1.436×10^{-5}	2.635×10^{-5}

[a.] Normalized Factor (nf) = (Desired technology node)/(Normalized Mean Node)

Future work includes consideration of additional IoT workload profiling use cases and honing of parameters to further refine the analytical models capable of predicting the benefits of CMOS-based alternatives for embedded IoT applications.

ACKNOWLEDGMENT

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