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Adaptive Non-Uniform Compressive Sensing using SOT-MRAM Multi-bit Precision Crossbar Arrays

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***Abstract*— A Compressive Sensing (CS) approach is applied to utilize intrinsic computation capabilities of Spin-Orbit Torque Magnetic Random Access Memory (SOT-MRAM) devices for IoT applications wherein lifetime energy, device area, and manufacturing costs are highly-constrained while the sensing environment varies rapidly. In this manuscript, we propose the Adaptive Compressed-sampling via Multi-bit Crossbar Array (ACMCA) approach to intelligently generate the CS measurement matrix using a multi-bit SOT-MRAM crossbar array. SPICE circuit and MATLAB algorithm simulation results indicate that ACMCA reduces reconstruction error by up to 4dB using a 4-bit quantized CS measurement matrix while incurring a negligible increase in the energy consumption of generating the matrix. Additionally, we introduce an algorithm called Energy-aware Adaptive Sensing for IoT (EASI) which determines the frequency of measurement matrix updates within the energy budget of an IoT device.**

***Index Terms*— Non-Uniform Compressive Sensing, Adaptive Compressive Sensing, SOT-MRAM, Crossbar Architecture.**

I. Introduction

In recent years, one of the main focuses of research in the Internet of Things (IoT) applications has been optimizing energy consumption while maximizing signal sampling performance and reconstruction accuracy [1], [2]. Recently, to decrease the energy consumption as well as storage needs and data transmission overheads, Compressive Sensing (CS) approaches are being investigated. Unlike conventional sampling methods that require the sampling to be performed at the Nyquist rate, CS algorithms aim to sample spectrally-sparse wide-band signals close to their information rate. Utilizing CS approaches help mitigate the overhead cost of sampling hardware [3], [4]. Non-uniform CS algorithms utilize Random Number Generator (RNG) for random sampling of the signal [4]. As opposed to True RNGs (TRNGs), Pseudo-RNGs (PRNGs) need to surmount challenges including limited quality of randomness, area utilization, and energy consumption overheads due to post-processing requirements [5], [6].

Thus, there is an increased demand for RNG circuits that are energy- and area-efficient and can provide adaptive behavior. Traditional implementation of non-uniform CS algorithms in hardware have been implemented using Complementary Metal Oxide Semiconductor (CMOS) technology [7], [8] and often result in inefficiencies in terms of area and power dissipation. Furthermore, recent advances in spintronics have enabled researchers to design TRNGs using Magnetic Tunnel Junctions (MTJs) [5], stochastic switching in MTJs using sub-threshold voltages [6], [9] precessional switching in MTJs [10], and Voltage-Controlled Magnetic Anisotropy (VCMA) MTJs [11]. However, all of these designs result in area footprint and energy consumption overheads due to their relatively complex hardware.

Herein, we devise a novel circuit-algorithm solution called *Adaptive Compressed-sampling via Multi-bit Crossbar Array (ACMCA)*, which utilizes a novel spin-based hardware circuit together with non-uniform compressive sensing algorithms to minimize energy consumption and area overheads while maximizing the sampling and reconstruction performance. The proposed ACMCA approach utilizes Spin Orbit Torque Magnetic Random Access Memory (SOT-MRAM) based multi-bit resistive devices to generate and store the CS measurement matrix elements. As developed herein, SOT-MRAM-based multi-bit resistive devices can attain a small area footprint and offer significant reduction in energy consumption [12]. Namely, to further leverage their intrinsic computationally ability in edge-based IoT application, SOT-MRAM-based Multi-bit Cells (SMCs) are utilized in a crossbar array fashion to perform Vector Matrix Multiplications (VMMs) required for sampling and reconstruction of the IoT signals.

The remainder of this paper is organized as follows: In Section II, background and related work are discussed and a detailed description of the SOT-MRAM-based multi-bit resistive devices utilized herein is provided. The proposed ACMCA approach is described in detail in Section III. Additionally, simulation results and comparisons are presented in Section IV. Finally, Section V concludes this manuscript.

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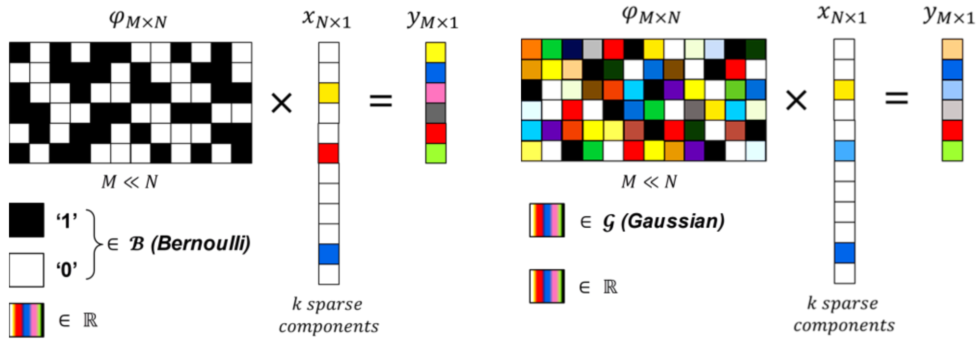


(a) (b)

Fig. 1: Compressive Sensing with a (a) Bernoulli measurement matrix and (b) Gaussian non-uniform measurement matrix.

II. Background and Related Work

A. Fundamentals of Compressive Sensing

Compressive Sensing (CS) techniques are designed to perform reconstruction algorithms to recover a k-sparse signal of length N using M measurements, with $M \ll N$. Based on the definition, a k-sparse signal has k non-zero entries in a given basis. Furthermore, the sparsity rate of the signal is defined as $(\frac{k}{N})$. Fundamentally, in order to sample the sparse signal vector, $x \in R^N$, we can use the measurement matrix, $\Phi \in R^{M\times N}$, and the relation $y = \Phi x$ to find the compressed measurements vector, $y \in R^M$. According to the literature, the sparse signal vector, $x \in R^N$, can be recovered from M measurements by solving the basis pursuit problem [13]:

$$\hat{x} = argmin \, \|x\|_1 \; s.t. \, y = \Phi x, \tag{1}$$

where $\|x\|_1 = \sum_i |x|$. It has been shown that $\hat{x}$ reconstructs the original signal vector if Φ satisfies a special condition known as the Restricted Isometry Property (RIP). An $M \times N$ matrix Φ satisfies RIP(p) if for any k-sparse vector x:

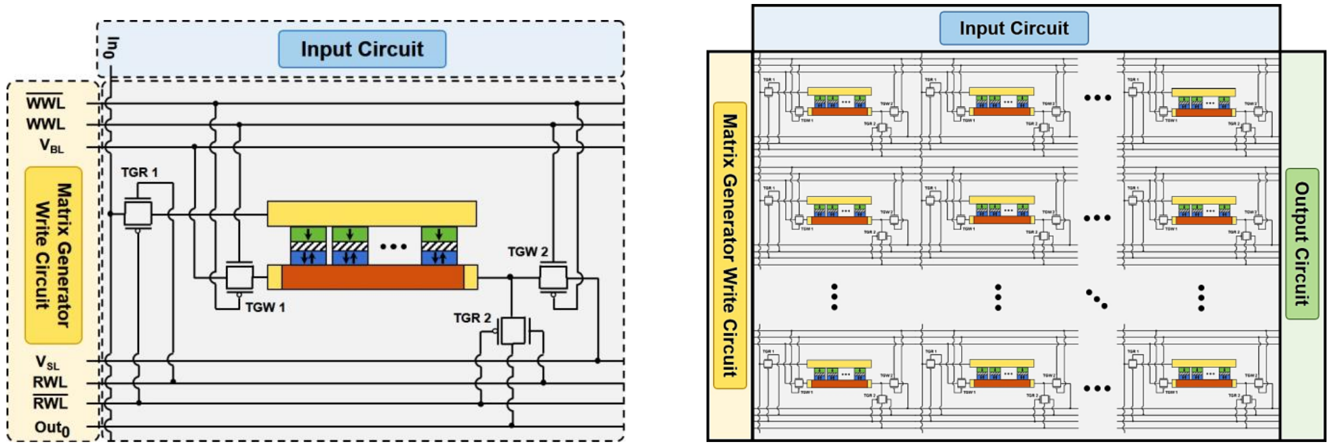
$$\|x\|_p(1-\delta) < \|\Phi x\|_p \leq \|x\|_p(1+\delta), \qquad 0 < \delta < 1. \tag{2}$$

Furthermore, the sparsity of the signal may be non-uniform and parts of the signal may carry more weight in the reconstruction accuracy, which are called Regions of Interest (RoI) [2]. Thus, it is crucial to employ an adaptive measurement matrix that is non-uniform and allows maximizing performance of reconstruction of the RoI parts of the signal that maintain higher sparsity rates. This is attained by sampling the RoI with higher frequency by adjusting the measurement matrix. Authors in [8] and [14] have verified that RIP condition is satisfied by non-uniform measurement matrices. Thus, non-uniform measurement matrices may be used for sparse signal sampling and reconstruction. Typically, non-uniform CS measurement matrix utilize Bernoulli and Gaussian distributions as shown in Fig. 1.

Spectrally sparse signals are utilized in many applications such as frequency hopping communications, musical audio signals, cognitive radio networks, and radar/sonar imaging systems [1]. As mentioned earlier, maximizing non-uniform CS reconstruction accuracy can be done through utilization of a measurement matrix that can adaptively change based on sparse input signal characteristics observed over time [2]. Recent achievements in high-performance sparse signal recovery algorithms utilizing adaptive measurement matrices have shown promising performance improvements [14]–[17]. However, they lack a feasible pathway to implement the algorithm within a hardware fabric considering the signal and hardware constraints or they require extensive hardware support to implement Adaptive Non-uniform CS (ANCS) techniques [2]. Additionally, previous CS hardware implementations incur significant overheads in terms of area footprint and energy consumption due to the use of a large number of CMOS transistors [7], [8]. Thus, in order to reduce area and energy consumption overheads, we devise a low-complexity hardware design.

B. SOT-MRAM-based Multi-bit Resistive Device

Recently, researchers have proposed use of multi-bit Voltage Controlled SOT-MRAM devices for dense memory system design [18], [19]. Although such devices offer energy-efficient write operation for dense memory systems, they incur overhead in terms of signaling and area. Thus, herein, we utilize the SOT-MRAM-based multi-bit resistive devices proposed in [12], which utilize the intrinsic probabilistic switching of nanomagnets while reducing signaling requirements compared to Voltage Controlled SOT-MRAM devices. The SOT-MRAM-based multi-bit resistive device provides a separate read and write path which will reduce the



(a) (b)

Fig. 2: Multi-bit stochastic SOT-MRAM-based (a) single cell, and (b) crossbar array.

read error rate, since write operation is performed using the spin Hall Effect (SHE) write mechanism [12]. Additionally, SOT-MRAM is expected to perform better in terms of endurance, power consumption, and speed [20]. The SMCs utilize the intrinsic probabilistic switching property of SOT-MRAM. Authors in [12] have fabricated and characterized an array of nanomagnets with Perpendicular Magnetic Anisotropy (PMA) located on a tantalum layer that acts as a SHE channel. Probabilistic switching of the individual nanomagnets is used to change the state of each SMC.

The total magnetization state of the nanomagnets in an SMC can be gradually increased or decreased by applying a proper current pulse through the tantalum layer. It is worth noting that the increase and decrease of the magnetization states of the SMCs is non-linear due to their stochastic nature. However, this can be addressed by modifying the amplitude and duration of the write current pulse applied. SOT switching of a fabricated Hall bar with a single nanomagnet is performed using current pulses of 50µs width in the presence of an in-plane external field of 20mT in the current direction. Note that the presence of an external magnetic field has been shown to not be a requirement for SOT driven switching of PMA nanomagnets [12].

Some of the SOT switching approaches used structures like wedges [21] or novel GSHE materials such as antiferromagnet PtMn [22] to eliminate the need for utilizing an external magnetic field. It has been demonstrated that a current pulse with width of 50µs can be applied to deterministically reset the state of all nanomagnets to -1. Moreover, a current with varying amplitudes is applied to probabilistically set the state of nanomagnets to +1. Note that higher current amplitude during the set operation will result in higher switching probability. Additionally, reducing the current pulse to 20µs will be required to increase the current amplitude. We can utilize 2^n nanomagnets operating in the probabilistic switching regime and working in parallel to design an n-bit SMC, where the resistances are calculated using (3).

$$\begin{aligned} &\textbf{\textit{for}}\ i = 1{:}(n+1)\ \textbf{\textit{do}} \\ &\qquad R_{SMC}(i) = R_P R_{AP} \,/\, (R_{AP}(n-(i-1)) + R_P(i-1)) \\ &\textbf{\textit{end}} \end{aligned} \tag{3}$$

III. Proposed Approach

Herein, we propose a novel MRAM-based Adaptive Non-uniform CS approach that utilizes the aforementioned multi-bit SOT-MRAM resistive devices. We utilize the SOT-MRAM based multi-bit crossbar array structure as shown in Fig. 2(b) to implement a CS algorithm. The SMCs shown in Fig. 2(a) are used within the crossbar array architecture to generate and store the measurement matrix, which is consisted of three main steps: reset, write, and read operations. In order to write into SMCs, first the write operation control signals, *WWL* and $\overline{WWL}$, enable the write transmission gates, *TGW1* and *TGW2*, which will connect the write path from bit line (*BL*) to source line (*SL*). Then, a write current will be applied with controlled pulses to enable probabilistic switching of the SMCs. To read the value stored in SMCs, the read operation control signals, *RWL* and $\overline{RWL}$, enable the read path from input port (*In*) to output port (*Out*), through the read transmission gates, *TGR1* and *TGR2*. After the read process, the measurement matrix elements can be modified via resetting the state of SMCs. This is performed similar to the write process except with a higher write current amplitude for deterministic switching.

According to the experimental results demonstrated in [12], the authors apply 20 current pulses with 6.97mA magnitude and 20µs width. In this approach, due to the probabilistic nature of switching of the SMC nanomagnets, depending on number of current pulses applied, magnitude of current, and width of pulses, only some of the nanomagnets may switch. Note that since all the current pulses have the same direction, they can only switch the nanomagnets from -1 to +1 state and once a nanomagnet is switched to +1, it will maintain that state in all subsequent current pulses. Herein, we devise a 4-bit SMC using MTJ devices instead of

Algorithm 1: Energy-aware Adaptive Sensing for IoT (EASI).

Input: Energy Threshold (γ), Energy Budget (EB), Critical Energy (CE), Matrix Generation Energy (MGE), Iteration *t-1* Matrix ($A_{t-1}(M, N)$), Iteration *t* Matrix Update (Φ), Update Frequency: Soft Threshold (α) and Hard Threshold (β) where $\alpha<\beta$
Output: Measurement Matrix of Iteration *t* ($A_t(M, N)$)

if $t == 1$ **then**
    $A_t(M, N) = \Phi$ /*Matrix Update*/
    $\gamma = \gamma - MGE$ /*Energy Threshold Update*/
else
    if $\gamma > EB$ **then**
        $A_t(M, N) = \Phi$ /*Matrix Update*/
        $\gamma = \gamma - MGE$ /*Energy Threshold Update*/
    if $CE < \gamma \leq EB$ **then**
        if $t \,\%\, \alpha == 0$ **then**
            $A_t(M, N) = \Phi$ /*Matrix Update*/
            $\gamma = \gamma - MGE$ /*Energy Threshold Update*/
        else $A_t(M, N) = A_{t-1}(M, N)$ /*No Matrix Update*/
    if $\gamma \leq CE$ **then**
        if $t \,\%\, \beta == 0$ **then**
            $A_t(M, N) = \Phi$ /*Matrix Update*/
            $\gamma = \gamma - MGE$ /*Energy Threshold Update*/
        else $A_t(M, N) = A_{t-1}(M, N)$ /*No Matrix Update*/
return $A_t(M, N)$

nanomagnets, where the overall resistance of the SMC is distributed between 1KΩ to 5KΩ.

As shown in Fig. 2, our proposed architecture offers control over the number of measurements and signal elements to provide flexibility to adjust to the signal characteristics such as sparsity rate, noise, etc. In particular, due to the non-volatility, zero leakage power dissipation, small area footprint, and instant-on operation features of the SMCs, the unused SMCs can be turned off while incurring nearly zero overhead in terms of energy consumption and area. Thus, we can modify the number of rows in the measurement matrix to increase the number of measurements in order to account for increased sparsity rate. Moreover, it becomes feasible to adjust the number of columns in the measurement matrix to increase the accuracy of the signal recovery.

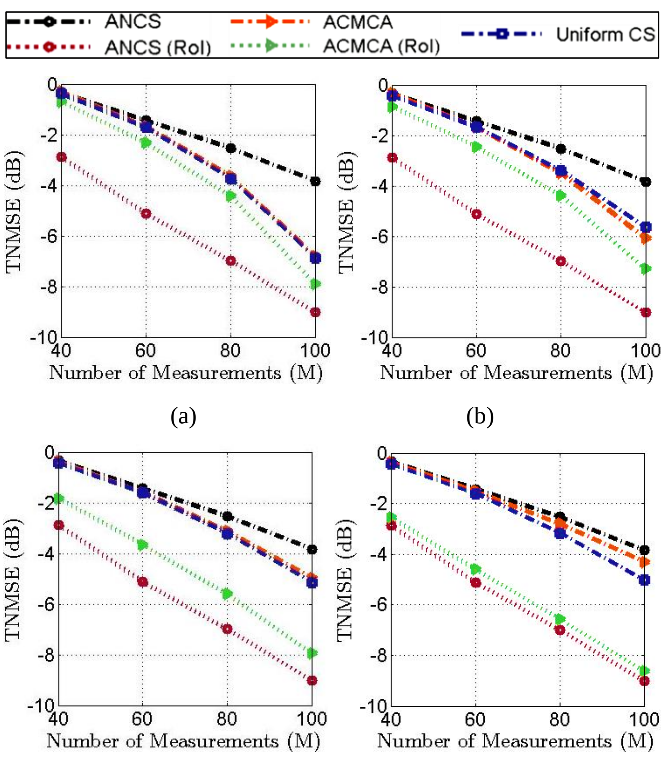


Fig. 3: TNMSE vs. Number of Measurements (M) for Accuracy Comparison of ANCS [2], ACMCA (Proposed), and Uniform CS, using (a) 1-bit, (b) 2-bit, (c) 3-bit, and (d) 4-bit measurement matrix.

Table 1: Comparison of single VMM operation's energy consumption in 4-bit CMOS Crossbar vs. SMC Crossbar.

Array Size (N×M)	CMOS Crossbar [27]	SMC Crossbar	Improvement
100×25	589 pJ	60 pJ	~9.8X
200×50	2,354 pJ	242 pJ	~9.7X
400×100	9,416 pJ	960 pJ	~9.8X

Moreover, the SMC crossbar is utilized to perform the VMMs required for compressive sampling and reconstruction of the IoT signals. In the SMC crossbar array, the number of input ports are equal to the number of signal elements while the number of output ports are equal to the number of measurements. Thus, VMM is performed by applying the input signal elements to the input ports of the SMC crossbar array, similar to the one shown in Fig. 2(a) as *In0*, and the result of the analog VMM for each measurement will be provided at the output ports of each row of the measurement matrix, similar to the one shown in Fig. 2(a) as *Out0*, where the outputs will be connected to a Winner Takes All (WTA) circuit in the output node. Furthermore, the number of signal elements and the number of measurements can be adaptively adjusted, which will enable the algorithm to adapt to the signal characteristics as well as the hardware constraints. In particular, the algorithm can trade off its reconstruction accuracy versus energy consumption by reducing the number of measurements or increase the number of measurements in case of high signal sparsity rate to maximize the reconstruction performance.

Additionally, Algorithm 1 demonstrates our proposed solution for CS measurement matrix update rule called *Energy-aware Adaptive Sensing for IoT (EASI)*, which considers the energy-budget of IoT devices. We introduce an update parameter in the algorithm presented in [15], [23] to modulate the frequency of updates to the measurement matrix while maintaining control over the energy consumption overhead. This parameter, which is defined herein as transportable metric called *Energy Threshold (γ)*, determines the update frequency of the measurement matrix and it is modified in each iteration according to the energy budget as shown in Algorithm 1. If γ is greater than the Energy Budget (EB), we will update the measurement matrix in every iteration of the algorithm. Moreover, if γ is less than the EB and greater than the Critical Energy (CE), we will reduce the frequency of updates to the measurement matrix by only updating the matrix every α iteration, where α is a soft update frequency threshold. Additionally, if γ is less than the CE, we will further decrease the frequency of updates made to the measurement matrix by updating it every β iteration, where β represents a strict threshold on the update rate. However, doing so might increase the overall reconstruction error rate. It is worth noting that the increase in the overall reconstruction error rate can be considered negligible since the reconstruction error rate of the RoI will still be reduced compared to uniform CS, which is the goal of the algorithm. Moreover, maximizing the update frequency of the measurement matrix will result in minimizing reconstruction error rate at the cost of increased energy consumption. This adaptive behavior will enable the designer to account for hardware constraints. Multi-objective optimization of energy parameters could be performed to improve performance while saving energy [24].

IV. SIMULATION RESULTS

We have performed SPICE circuit and MATLAB CS algorithm simulations to evaluate the behavior and efficiency of our proposed approach. We have used the 14nm FinFET PTM library [25], the Pin-Sim framework [26], and the SMC device simulation, demonstration, and experimental results provided in [12] in our simulations to validate the proposed ACMCA approach and extract area and energy consumption estimates. In particular, we utilize the scaled SMC device parameters within Pin-Sim to simulate the SMC crossbar array. According to our results, energy consumption estimates for VMM using an SMC crossbar array to implement our modified version of the CS algorithm introduced in [15], [23] using a variety of N and M values compared to CMOS crossbar array [27] are listed in Table 1. As shown in Table 1, utilizing the SMC crossbar array for VMM operation provides nearly 10-fold energy consumption reduction compared to a CMOS crossbar array. Write energy consumption estimates for populating the measurement matrix are 3nJ for N×M=100×25, 12nJ for N×M=200×50, and 50nJ for N×M=400×100, on average.

Furthermore, using the intrinsic probabilistic behavior of SMCs, ACMCA eliminates need for TRNG circuits, which are usually bulky and consume a significant amount of energy when implemented in CMOS. ACMCA using N×M=400×100 increases energy consumption by 7-fold on average to populate the measurement matrix. However, the measurement matrix is populated infrequently and once an estimate of the RoI is achieved, there will only be small updates to a few SMCs and not the entire matrix. Thus, the energy consumption overhead of populating the measurement matrix can be considered negligible. Moreover, according to transistor count, our proposed approach achieves a ~26-fold device reduction compared to CMOS crossbar.

V. CONCLUSION

Herein, a spin-based non-uniform compressive sensing circuit-algorithm approach is developed to consider the signal dependent constraint as well as hardware limitations called *Adaptive Compressed-sampling via Multi-bit Crossbar Array (ACMCA).* ACMCA circuit-algorithm simulation results indicate a reduced reconstruction error by up to 4dB compared to Uniform CS methods while offering nearly 10-fold reduction in energy consumption for performing VMM compared to a CMOS-based crossbar. Moreover, we introduce the *Energy-aware Adaptive Sensing for IoT (EASI)* algorithm, which considers the energy budget when updating the CS measurement matrix to reduce energy consumption of the IoT device at the cost of slight loss in accuracy. Due to infrequent updates of the measurement matrix, energy consumption overhead of populating the matrix can be considered negligible.

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