

# AQuRate: MRAM-based Stochastic Oscillator for Adaptive Quantization Rate Sampling of Sparse Signals

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## ABSTRACT

Recently, the promising aspects of compressive sensing have inspired new circuit-level approaches for their efficient realization within the literature. However, most of these recent advances involving novel sampling techniques have been proposed without considering hardware and signal constraints. Additionally, traditional hardware designs for generating non-uniform sampling clock incur large area overhead and power dissipation. Herein, we propose a novel non-uniform clock generator called Adaptive Quantization Rate (AQR) generator using Magnetic Random Access Memory (MRAM)-based stochastic oscillator devices. Our proposed AQR generator provides  $\sim 25$ -fold reduction in area, on average, while offering  $\sim 6$ -fold reduced power dissipation, on average, compared to the state-of-the-art non-uniform clock generators.

## CCS CONCEPTS

• **Hardware**  $\rightarrow$  **Data conversion; Spintronics and magnetic technologies; Emerging architectures;**

## KEYWORDS

Analog to Digital Converter, Adaptive Sampling Rate, Non-uniform Clock Generator, MRAM-based Stochastic Oscillator, Compressive Sensing.

## 1 INTRODUCTION

Recently, non-uniform sampling approaches such as Compressive Sensing (CS) have been proposed to reduce the energy consumption of sampling operation by reducing number of samples in each frame, reduce required storage to save the sampled data, and reduce the data transmission due to lower number of samples taken [15, 19, 20]. Additionally, event-driven sampling, such as level-crossing sampling, has been widely adopted as a promising CS technique to maximize the performance of sampling operation while reducing energy consumption [18]. Furthermore, CS techniques are utilized to sample spectrally sparse wide-band signals close to their information rate rather than their Nyquist rate, which can be a challenge using conventional uniform sampling techniques due to the high cost of the hardware that is capable of performing the sampling operation at a high Nyquist rate.

Despite all the benefits that CS techniques offer, they are typically realized oblivious to the hardware limitations such as energy, bandwidth, and battery capacity. Additionally, signal-dependent constraints such as sparsity and noise level are ignored while studying the quantization rate and resolution trade-off. The aforementioned hardware-dependent and signal-dependent constraints alter during the sampling operation. Thus, an adaptive quantization rate and resolution optimization circuitry is required to maximize sampling performance while minimizing the number of samples to

reduce energy consumption, data transmission, and storage. Adaptive quantization rate and resolution sampling might be readily achieved from the algorithm perspective, however it requires a hardware platform that is capable of real-time adaptation according to certain signal behavior such as sparsity rate. Recently, an adaptive optimization of the quantization rate and resolution during signal acquisition has been investigated in [14].

Previous works on adaptive quantization rate and resolution ADCs have been implemented using Complementary Metal Oxide Semiconductor (CMOS) technology and considering a low-pass signal model [3, 18]. Herein, we propose a spin-based Adaptive quantization rate (AQR) generator circuit that considers the signal dependent constraint as well as hardware limitations. The proposed AQR generator circuit utilized Magnetic Random Access Memory (MRAM)-based stochastic oscillator devices, which offer miniaturization and significant energy savings [6].

## 2 BACKGROUND AND RELATED WORK

Recently researchers have achieved significant performance improvements using sparse signal recovery techniques. Spectrally sparse signals are utilized in many applications such as frequency hopping communications, musical audio signals, cognitive radio networks, and radar/sonar imaging systems [14]. Additionally, a major challenge in spectrum sensing is that in most cases, the sparse components of the signal are spread over a wide-band spectrum and need to be acquired without prior knowledge of their frequencies. Moreover, spectrum-aware communication networks require Radio Frequency and mixed-signal hardware architectures that can achieve very wide-band but energy-efficient spectrum sensing [14].

The cornerstone to achieving CS approaches and non-uniform sampling techniques is the utilization of an asynchronous pseudo-random clock generator, usually referred to as non-uniform clock generator, which is consisted of a Linear Feedback Shift Register (LFSR) that selects a clock signal at random from a series of ring oscillators with different frequency and phases [3, 4, 10, 11, 13]. In most cases, these circuits require a large number of CMOS transistors and incur significant area overhead and power dissipation. Recently, a novel approach for generating the non-uniform clock using VCMA-MTJ devices is proposed in [11] and the authors have shown that their proposed design can achieve significant area and power dissipation reduction compared to the previous CMOS-based pseudo-random clock generators. However, the authors in [11] considered the frequency of the signal in order to generate the sampling clock, which limits the bandwidth and in case of spectrally sparse signals, where no prior knowledge of frequency is available, their proposed approach will face challenges. Herein, we consider the sparsity rate of the signal to generate the sampling clock. This will minimize the number of samples and results in more energy savings.

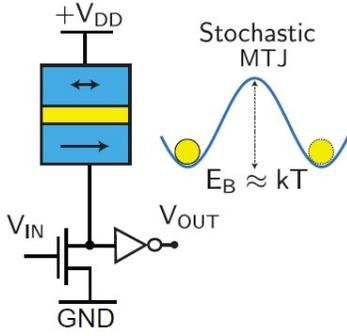


Figure 1: The building block of the proposed spin-based AQR generator [6].

Furthermore, our proposed design has reduced complexity compared to other designs proposed in the literature due to significant reduction in the CMOS circuit elements.

### 3 ADAPTIVE QUANTIZATION RATE GENERATOR

#### 3.1 MRAM-based Stochastic Device as a Building Block for AQR generator

In this section, we show that a recently proposed building block with embedded MRAM technology can enable the hardware realization of an AQR generator. The structure of the MRAM-based stochastic device is shown in Fig. 1, which includes a magnetic tunnel junction (MTJ) that is a 2-terminal device with two different resistive levels depending on the orientation of its ferromagnetic (FM) layers, called *fixed layer* and *free layer*. The fixed layer is designed to have a fixed magnetic orientation, while the magnetization orientation of the free layer can be switched. In MRAM-based memory devices, a thermally-stable nanomagnet with a large energy barrier with respect to the thermal energy ( $kT$ ) is utilized for free layer so that the fixed layer can function as a non-volatile memory. In recent years the use of superparamagnetic MTJs that are not thermally stable have been experimentally and theoretically investigated in search of functional spintronic devices [5, 7–9, 12, 17, 21, 22].

In this paper, we use an MRAM device with a low energy-barrier nanomagnet ( $E_B \ll 40kT$ ), which is thermally unstable [6]. The resistance of an MTJ with such a low energy barrier nanomagnet randomly fluctuates between high ( $R_{AP}$ ) and low resistance states ( $R_P$ ). This creates a fluctuating output voltage at the drain of the NMOS transistor, which can be amplified by an inverter circuit to produce a stochastic output that can be modulated by the input voltage. In particular, the output voltage at the drain of the NMOS transistor can be shorted to the ground by reducing its drain-source resistance ( $r_{ds}$ ) through increasing the input voltage ( $V_{IN}$ ), or it can be near  $V_{DD}$  by increasing the  $r_{ds}$  through decreasing  $V_{IN}$ . The device operation can be comprehended by considering the MTJ conductance [6]:

$$G_{MTJ} = G_0 \left[ 1 + m_z \frac{TMR}{(2 + TMR)} \right] \quad (1)$$

where  $m_z$  is the free layer magnetization that is stochastically fluctuating due to the thermal noise,  $G_0$  is the average MTJ conductance,  $(G_P + G_{AP})/2$ , and  $TMR$  is the tunneling magnetoresistance ratio. The drain voltage can be expressed as:

$$V_{DRAIN}/V_{DD} = \frac{(2 + TMR) + TMR m_z}{(2 + TMR)(1 + \alpha) + TMR m_z} \quad (2)$$

where  $\alpha$  is the ratio of the transistor conductance ( $G_T$ ) to the average MTJ conductance ( $G_0$ ). The maximum fluctuations at the drain occurs when  $\alpha \approx 1$ , thus the MTJ resistance is approximately equal to the NMOS resistance when  $V_{IN} = 0.5V_{DD}$ . Since the drain voltage fluctuations are in the order of hundreds of mV for typical TMR values, an additional inverter is used to amplify the noise to produce output voltages ranging from 0 to  $V_{DD}$ .

#### 3.2 AQR Generator Circuit

To realize an effective hybrid emerging device and CMOS circuit, one useful approach can be to consider stochastic and deterministic attributes separately. For instance, Fig. 2 depicts the proposed AQR generator circuit wherein a 2-terminal MTJ realizes stochastic behavior to provide the non-uniform clock generation capability.

The quantized Sparsity Rate Estimator (SRE) module shown in Fig. 2 estimates the sparsity rate of the digital output bit-stream by estimating the sparse spectral components of the digital output using an iterative algorithm. Recently, rapid and optimized sparse component estimation method is proposed in [14]. In the approach proposed in [14] in order to minimize the computational complexity of the sparse component estimation, an sliding window approach is utilized and the algorithm operates only one iteration on each frame of the input by utilizing the previous estimate as an initial value. This will result in gradual convergence of the sparse components to the actual values across iterations. These algorithms can be employed to find the sparsity rate of the signal. In most cases, sparsity rate of analog signals, which can be described as the number of non-zero elements in divided by the total number of elements the sparse representation of the signal, is between 5% to 15% in many applications including those targeted herein.

When the SRE module estimates the sparsity rate of the signal based on the digital output of the previous frame, it will then generate a voltage level according to that sparsity rate of the input analog signal. This voltage, referred to as  $V_{SR}$ , will be applied to the gate of the NMOS transistor shown in Fig. 2 and results in an stochastic bit-stream generated by the MRAM-based stochastic oscillator device. The stochastic bit-stream output generated by the MRAM-based stochastic oscillator device will be forwarded to the D-Flip-Flop (D-FF) as shown in Fig. 2 and the result of the 2-input NAND gate between the output of the D-FF and the actual clock of the circuit will generate the required quantization rate to be used for the following frame of the signal acquisition, referred to as Asynchronous Clock (A-Clk) in Fig. 2. Additionally, the SRE module can also be used by the recovery algorithms to efficiently recover the sampled signal [14]. Additionally, the A-Clk will be forwarded to the sparse recovery algorithm to provide necessary information about the samples taken from the signal to assist with the signal reconstruction.

To obtain the relation between the output probability of the stochastic MRAM-based AQR generator and its input voltage, we

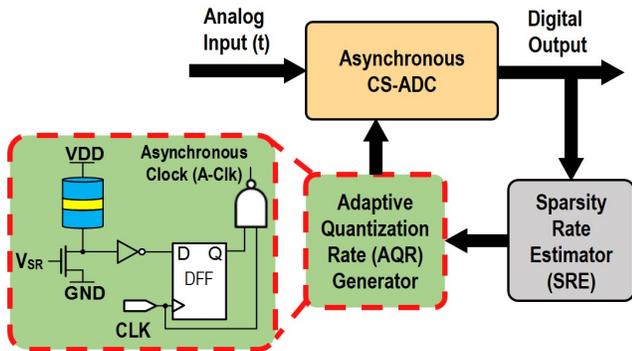


Figure 2: Integration of AQR generator circuit within the Compressive Sensing ADC (CS-ADC) system design.

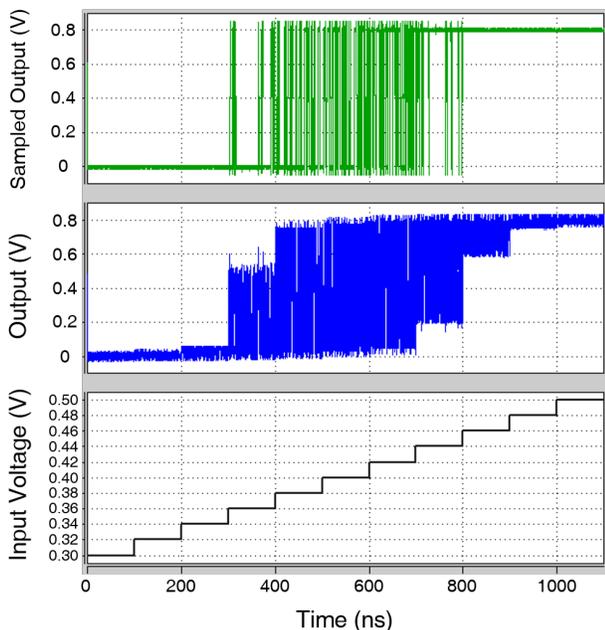


Figure 3: The sampled output of the stochastic MRAM-based building block for AQR generator for various input voltages.

have applied an input pulse that its amplitude starts from  $GND$  and is increased by  $200mV$  every  $100ns$  until it reaches  $V_{DD}$ . The output of the building block is sampled with a  $1GHz$  clock frequency using a D-FF circuit, as shown in Fig. 3.

#### 4 SIMULATION RESULTS

In order to evaluate and validate the behavior and functionality of the proposed AQR generator circuit, SPICE and MATLAB simulations were performed. We have utilized the  $14nm$  High Performance FinFET Predictive Technology Model (PTM) [2] as well as the MRAM-based stochastic oscillator device model and parameters represented in [6] to implement and evaluate the proposed AQR generator circuit.

Table 1: Comparison with recently proposed non-uniform clock generator designs

Design	Technology ( $V_{nominal}$ )	$Power_{norm}$	$Area_{norm}$
[11]	65nm (1.1V)	$\sim 1\times$	$\sim 1\times$
[13]	65nm (1.1V)	$\sim 2\times$	$\sim 21\times$
[4]	90nm (1.2V)	$\sim 2\times$	$\sim 51\times$
[3]	28nm (1.0V)	$\sim 18\times$	N/A
This Work	14nm (0.8V)	$1\times$	$1\times$

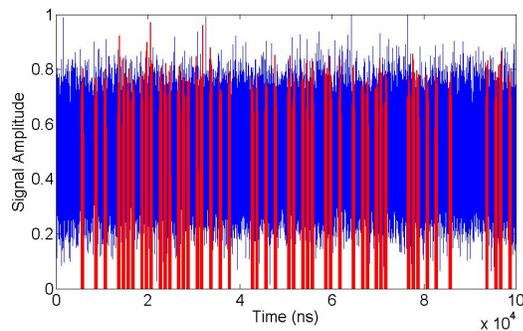
According to our results, AQR provides significant power dissipation and area reductions compared to the state-of-the-art nonuniform clock generators listed in Table 1 [3, 4, 11, 13]. According to our simulation results, power dissipation of the proposed AQR generator circuit is  $22.64\mu W$  on average. With respect to area utilization, our proposed AQR design requires only 23 FinFET transistors, which attains a significant reduction in the transistor count and complexity of the non-uniform clock generator circuit present in state-of-the-art designs [3, 4, 11, 13]. Thus, AQR avoids high transistor counts while making it unnecessary to use of large LFSR circuits that contain numerous D-FFs as well as several logic gates and multiplexers. For a more equitable comparison in terms of area and power dissipation, we have derived (3) and (4) considering General Scaling method [16] to normalize the power dissipation and area of the designs listed in Table 1. Based on the General Scaling method, voltage and area scale at different rate of  $U$  and  $S$ , respectively. Thus, the power dissipation is scaled with respect to  $1/U^2$  and area per device is scaled according to  $1/S^2$  [16].

$$Power_{norm} = \frac{Power_x}{Power_{AQR}} \times \left(\frac{1}{U}\right)^2 = \frac{Power_x}{Power_{AQR}} \times \left(\frac{0.8V}{V_{nominal}}\right)^2 \quad (3)$$

$$Area_{norm} = \frac{Area_x}{Area_{AQR}} \times \left(\frac{1}{S}\right)^2 = \frac{Area_x}{Area_{AQR}} \times \left(\frac{14nm}{Technology}\right)^2 \quad (4)$$

where,  $V_{nominal}$  is the nominal voltage of the technology model,  $Technology$  refers to the technology node in nanometers, and subscript  $x$  refers to the design that we want to scale its power dissipation and area according to the technology models. According to (3) and (4), AQR provides power dissipation reduction up to one-order-of-magnitude compared to the state-of-the-art nonuniform clock generators as listed in Table 1. Additionally, AQR offers up to one-orders-of-magnitude area reduction compared to the designs provided in Table 1 using the scaling comparison trends accepted in the literature.

As described in Section 3.2, sparsity rate of analog signals is usually within the range of  $5\% - 15\%$ . Fig. 4 depicts an example output of the AQR generator for sampling of a sparse signal with  $5\%$  sparsity rate. Moreover, we have embedded our proposed AQR generator within CS recovery algorithms called Orthogonal Matching Pursuit (OMP) and Compressive Sampling Pursuit (CoSaMP) [1] in order to evaluate the architectural simulation results and in order to recover the signal from the samples taken using the AQR



**Figure 4: Sampling an analog signal with sparsity rate of 5% using AQR generator. Blue represents the signal and Red represents the samples taken using the AQR generator.**

generator. According to the results, the mean normalized errors of the reconstruction of the signals with 5%, 10%, and 15% sparsity rates using OMP are 0.0504, 0.0446, and 0.0252, respectively. Moreover, the mean normalized errors of the reconstruction of the signals with 5%, 10%, and 15% sparsity rates using CoSaMP are 0.0487, 0.0304, and 0.0245, respectively.

## 5 CONCLUSIONS

We have devised a novel non-uniform clock generator called Adaptive quantization rate (AQR) generator using MRAM-based stochastic oscillator devices. Our proposed AQR generator considers signal constraints, such as sparsity rate, as well as hardware constraints, such as area and power dissipation, in order to generate the non-uniform clock for the asynchronous CS-ADC. Compared to similar non-uniform clock generators presented in the literature, AQR generator provides significant area reduction of  $\sim 25$ -fold on average, while achieving power dissipation reduction of  $\sim 6$ -fold, on average.

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## REFERENCES

- [1] 2009. CoSaMP: Iterative signal recovery from incomplete and inaccurate samples. *Applied and Computational Harmonic Analysis* 26, 3 (2009), 301–321.
- [2] Arizona State University (ASU). [n. d.]. 14nm HP-FinFET Predictive Technology Model (PTM), accessed on 26 November 2018, available at: <http://ptm.asu.edu/>. ([n. d.]). <http://ptm.asu.edu/>
- [3] David Bellasi, Luca Bettini, Thomas Burger, Qiting Huang, Christian Benkeser, and Christoph Studer. 2014. A 1.9 GS/s 4-bit sub-Nyquist flash ADC for 3.8 GHz compressive spectrum sensing in 28 nm CMOS. In *2014 IEEE 57th International*

- Midwest Symposium on Circuits and Systems (MWSCAS)*. IEEE, 101–104. <https://doi.org/10.1109/MWSCAS.2014.6908362>
- [4] Rashed Zafar Bhatti, Keith M. Chugg, and Jeff Draper. 2007. Standard cell based pseudo-random clock generator for statistical random sampling of digital signals. In *2007 50th Midwest Symposium on Circuits and Systems*. IEEE, 1110–1113. <https://doi.org/10.1109/MWSCAS.2007.4488752>
- [5] Kerem Yunus Camsari, Rafatul Faria, Brian M Sutton, and Supriyo Datta. 2017. Stochastic p-bits for invertible logic. *Physical Review X* 7, 3 (2017), 031014.
- [6] Kerem Yunus Camsari, Sayeef Salahuddin, and Supriyo Datta. 2017. Implementing p-bits with embedded mtj. *IEEE Electron Device Letters* 38, 12 (2017), 1767–1770.
- [7] Won Ho Choi, Yang Lv, Jongyeon Kim, Abhishek Deshpande, Gyuseong Kang, Jian-Ping Wang, and Chris H Kim. 2014. A magnetic tunnel junction based true random number generator with conditional perturb and real-time output probability tracking. In *Electron Devices Meeting (IEDM), 2014 IEEE International*. IEEE, 12–5.
- [8] Punyashloka Debashis, Rafatul Faria, Kerem Y Camsari, Joerg Appenzeller, Supriyo Datta, and Zhihong Chen. 2016. Experimental demonstration of nanomagnet networks as hardware for ising computing. In *Electron Devices Meeting (IEDM), 2016 IEEE International*. IEEE, 34–3.
- [9] Akio Fukushima, Takayuki Seki, Kay Yakushiji, Hitoshi Kubota, Hiroshi Imamura, Shinji Yuasa, and Koji Ando. 2014. Spin dice: A scalable truly random number generator based on spintronics. *Applied Physics Express* 7, 8 (2014), 083001.
- [10] Selcuk Kose, Emre Salman, Zeljko Ignjatovic, and Eby G. Friedman. 2008. Pseudo-random clocking to enhance signal integrity. In *2008 IEEE International SOC Conference*. IEEE, 47–50. <https://doi.org/10.1109/SOCC.2008.4641477>
- [11] H Lee, C Grezes, A Lee, F Ebrahimi, P Khalili Amiri, and K L Wang. 2017. A Spintronic Voltage-Controlled Stochastic Oscillator for Event-Driven Random Sampling. *IEEE Electron Device Letters* 38, 2 (2017), 281–284. <https://doi.org/10.1109/LED.2016.2642818>
- [12] Nicolas Locatelli, Alice Mizrahi, A Accioly, Rie Matsumoto, Akio Fukushima, Hitoshi Kubota, Shinji Yuasa, Vincent Cros, Luis Gustavo Pereira, Damien Querlioz, et al. 2014. Noise-enhanced synchronization of stochastic magnetic oscillators. *Physical Review Applied* 2, 3 (2014), 034009.
- [13] Muhammad Osama, Lamya Gaber, and Aziza Hussein. 2016. Design of high performance Pseudorandom Clock Generator for compressive sampling applications. In *2016 33rd National Radio Science Conference (NRSC)*. IEEE, 257–265. <https://doi.org/10.1109/NRSC.2016.7450836>
- [14] Soheil Salehi, Mahdi Boloursaz Mashhadi, Alireza Zaeemzadeh, Nazanin Rahnavard, and Ronald F. De Mara. 2018. Energy-Aware Adaptive Rate and Resolution Sampling of Spectrally Sparse Signals Leveraging VCMA-MTJ Devices. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (2018), 1–1. <https://doi.org/10.1109/JETCAS.2018.2857998>
- [15] Shiram Sarvotham, Dror Baron, Richard G. Baraniuk, Shiram Sarvotham, Dror Baron, and Richard G. Baraniuk. 2006. Measurements vs. Bits: Compressed Sensing meets Information Theory. *Allerton Conference on Communication, Control and Computing* (9 2006). <https://scholarship.rice.edu/handle/1911/20323>
- [16] Aaron Stillmaker and Bevan Baas. 2017. Scaling equations for the accurate prediction of CMOS device performance from 180Ånm to 7Ånm. *Integration* 58 (6 2017), 74–81. <https://doi.org/10.1016/J.VLSI.2017.02.002>
- [17] Brian Sutton, Kerem Yunus Camsari, Behdash Behin-Aein, and Supriyo Datta. 2017. Intrinsic optimization using stochastic nanomagnets. *Scientific reports* 7 (2017), 44370.
- [18] Tzu-Fan Wu, Cheng-Ru Ho, and Mike Shuo-Wei Chen. 2017. A Flash-Based Non-Uniform Sampling ADC With Hybrid Quantization Enabling Digital Anti-Aliasing Filter. *IEEE Journal of Solid-State Circuits* 52, 9 (2017), 2335–2349. <https://doi.org/10.1109/JSSC.2017.2718671>
- [19] Alireza Zaeemzadeh, Jamie Haddock, Nazanin Rahnavard, and Deanna Needell. 2018. A Bayesian Approach for Asynchronous Parallel Sparse Recovery. In *52nd Asilomar Conference on Signals, Systems, and Computers*. IEEE, Pacific Grove, CA, 1980–1984. <https://doi.org/10.1109/ACSSC.2018.8645176>
- [20] Alireza Zaeemzadeh, Mohsen Joneidi, and Nazanin Rahnavard. 2017. Adaptive non-uniform compressive sampling for time-varying signals. IEEE, 1–6. <https://doi.org/10.1109/CISS.2017.7926148>
- [21] Ramtin Zand, Kerem Y Camsari, Supriyo Datta, and Ronald F DeMara. 2018. Composable Probabilistic Inference Networks Using MRAM-based Stochastic Neurons. *arXiv preprint arXiv:1811.11390* (2018).
- [22] Ramtin Zand, Kerem Yunus Camsari, Steven D. Pyle, Ibrahim Ahmed, Chris H. Kim, and Ronald F. DeMara. 2018. Low-Energy Deep Belief Networks Using Intrinsic Sigmoidal Spintronic-based Probabilistic Neurons. In *Proceedings of the 2018 on Great Lakes Symposium on VLSI (GLSVLSI '18)*. ACM, Chicago, IL, USA, 15–20. <https://doi.org/10.1145/3194554.3194558>